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RTL9303-CG

LAYER 3 MANAGED 8*10G PORT SWITCH CONTROLLER

DATASHEET

(CONFIDENTIAL: Development Partners Only)

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USING THIS DOCUMENT

This document is intended for the hardware and software engineer's general information on the Realtek RTL9303 chip.

Though every effort has been made to ensure that this document is current and accurate, more information may have become available subsequent to the production of this guide.

ELECTROSTATIC DISCHARGE (ESD) WARNING

This product can be damaged by Electrostatic Discharge (ESD). When handling, care must be taken. Damage due to inappropriate handling is not covered by warranty.

Do not open the protective conductive packaging until you have read the following, and are at an approved anti-static workstation.

- Use an approved anti-static mat to cover your work surface.
- Use a conductive wrist strap attached to a good earth ground
- Always discharge yourself by touching a grounded bare metal surface or approved anti-static mat before picking up an ESD-sensitive electronic component
- If working on a prototyping board, use a soldering iron or station that is marked as ESD-safe
- Always disconnect the microcontroller from the prototyping board when it is being worked on

REVISION HISTORY

Revision	Release Date	Summary
1.0	2018/03/30	First release.
1.1	2018/06/29	Corrected minor typing errors. Deleted pin descriptions regarding unused pins.
1.1-1	2018/9/5	Change SDS 10GBase-R $V_{TX\text{-}DIFFp\text{-}p}$ 900mV->1200mV Update master SPI timing Corrected minor typing errors.

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1. General Description

The Realtek RTL9303-CG is a highly integrated Layer3 switch supporting Energy Efficient Ethernet (EEE). It has up to 8-ports*10G Ethernet MAC.

The RTL9303 is embedded with an up to 800MHz MIPS-34Kc CPU. It supports a Maximum 64Mbyte SPI NOR Flash, and 1G-Byte DDR3 SDRAMs (maximum). An embedded 64KB SRAM can be used for time-sensitive applications. For connecting to an external CPU, it supports the SGMII interface.

The RTL9303 has a 4K-entry VLAN table. It provides VLAN classification according to port-based, protocol-and-port-based, MAC-based, IP-subnet-based, Ingress VLAN translation and Flow-based capability. It also supports IVL (Independent VLAN Learning), SVL (Shared VLAN Learning), and IVL/SVL (both Independent and Shared VLAN Learning) for flexible network topology architecture. In network access applications it provides IEEE802.1ad (Q-in-Q) for double tag insertion and removal function. In addition, VLAN translation function is also supported for Metro Ethernet applications.

The RTL9303 supports 16K entries in a L2 MAC table with 2-left 4-way hashing algorithm. An independent 1K-entry Forwarding table is used to support Multicast functions, such as IGMP snooping.

The RTL9303 supports a 2K-entry VLAN/Ingress Access Control List (ACL). The ACL function supports L2/L3/L4 in IPv4/IPv6 protocols and performs configurable actions, such as Drop/Permit/Redirect/ Copy/Unicast Routing/Mirror/Logging/Policing/Ingress VLAN conversion/Egress VLAN conversion/QoS remarking/ VLAN tag status assignment. The RTL9303 supports per-port ingress/egress bandwidth control and per-queue egress bandwidth control.

L3 routing supports IPv4 unicast routing, IPv6 unicast routing, IPv4 multicast routing and IPv6 multicast routing. Routing table is mainly composed of L3 host table and L3 LPM table. L3 host table is shared by IPUC and IPMC, and is 2-left 6-way host table. Routing is the process of forwarding packets hop by hop on layer3. It primarily includes finding an outgoing interface and a next hop, modifying the packets' SMAC, DMAC, VID (if provided), TTL, and L3 header checksum (for IPv4) and forwarding. The RTL9303 supports strict and loose uRPF.

The RTL9303 provides three types of packet scheduling, including SP (Strict Priority), WFQ (Weighted Fair Queuing), and WRR (Weighted Round Robin). Each port has 8 physical queues and each queue provides a leaky-bucket to shape the incoming traffic into the average rate behavior. The Broadcast/Multicast/Unknown-Multicast/Unknown-Unicast storm suppression function can inhibit external and internal malicious attacks.

The RTL9303 supports 4-sets of port mirror configurations to mirror ingress and egress traffic. RSPAN and sFlow are also supported for traffic monitoring purposes. For network management purposes, complete MIB counters are supported to provide forwarding statistics in real time. The Link aggregation function enhances link redundancy and increases bandwidth linearly.

2. Features

- Hardware Interface
  - 160Gbps switch capacity
  - Flexible interfaces for internal or external CPU; either one can be enabled
    - Port 28 SGMII interface or Port 27 10G-R/ USXGMII/ HISGMII/ 1000BASE-X/SGMII interface for external CPU
    - Supports SPI interface for external CPU to access internal register
  - Maximum 64 Mbyte SPI NOR Flash or 512MB SPI NAND Flash and maximum 1GB DDR3 SDRAMs for internal MIPS-34Kc
  - Supports flash-only solution
    - Single/Dual/Quad SPI flash
    - 64Kbyte SP-SRAM
  - Supports USB2.0 host
  - Embedded MIPS-34Kc with MMU
    - MIPS32 instruction set and 9-stage pipeline
    - Up to 800MHz CPU clock rate
    - 32Kbyte I-Cache and 32Kbyte D-Cache
    - 32 TLB entry
    - Two UART interfaces to control internal CPU with Command Line Interface (CLI)
  - Supports 8-set I2C master and 2-set SPI master
- VLAN Function
  - Supports IVL, SVL, and IVL/SVL
  - Supports IEEE 802.1Q VLAN and Q-in-Q VLAN
    - 4K-entry VLAN Table
    - Supports up to 64 spanning tree instances for MSTP (IEEE 802.1s), RSTP (IEEE 802.1w), and STP (IEEE 802.1D)
    - Forwarding bases on inner or outer VLAN
    - Ingress/Egress VLAN filtering per-port based
    - Per ingress port and per-tag-status select forwarding VID source
  - Port-based/Port-and-protocol-based /MAC-based/IP-Subnet-based/Flow-based VLAN
  - VLAN Conversion Table
    - 1024 ingress and 512 egress table
    - Specific VLAN or a VLAN range to convert
    - Shift operation is supported
    - Selective Q-in-Q
- L2 MAC Function
  - 16K-entry L2 MAC table
    - 2-left 4-way hashing algorithm
    - 2 hash algorithm selection for L2 table searching/learning
    - Source/Destination MAC filtering
    - Per port enables aging
  - Independent 1K entry Multicast table for L2/IP Forward function
  - 12Mbit SRAM Packet Buffer
  - Jumbo frame up to 12KB
  - Supports 48 Reserved Multicast Addresses processing
  - Limited learned L2 MAC entry on Port/VLAN/System
  - MAC address Aging-out and New-learn notification

- L2 Miscellaneous Functions
  - Supports broadcast/multicast/unknown-multicast/unicast/unknown-unicast packet suppression control in pps/bps mode
  - Supports Port Mirroring/Sampling
    - Supports 4 sets of mirror configuration
    - Supports flow-based mirror
    - RSPAN mirror
    - sFlow sampling
  - Supports Link Aggregation (IEEE 802.3ad) for 64 groups of link aggregators with up to 8 ports per-group
    - Hardware trunk fail-over
    - Distribution algorithm can be based on SPP, SMAC, DMAC, VLAN ID, SIP, DIP, L4 source port, L4 destination port, Protocol ID and IPv6 Flow Label
    - Known multicast/flooding packets can be separated
  - Traffic isolation function to enhance port security
  - Attack Prevention
    - LAND attack
    - Blat attack
    - TCP control flag attack
    - Ping attack
    - Packet length attack
  - OAM
    - 802.3ah OAM loopback
    - 802.3ah Dying Gasp
- L3 Functions
  - IPv4/IPv6 unicast routing
    - 64 Router MAC
    - 6K-entry host table (6K IPv4/2K IPv6)
    - 2-left 6-way host table
    - 2 hash algorithm selection for host table searching
    - 512-entry LPM (Longest Prefix Match) table(512 IPv4/128 IPv6)
    - 2K next hop table
    - 128 Egress L3 interfaces
    - Supports uRPF (unicast Reverse Path Forwarding)
    - Supports PBR (Policy-Based Routing)
  - IPv4/IPv6 multicast routing
    - Routing entry shared with ip unicast host table
    - 512 L3 OIL (Outgoing Interface List) list for multicast replication
    - 1K forward table entry
    - Supports multicast (S, G, V) or (*, G, V) routing/bridging
    - Supports multicast (S, G) or (*, G) bridging/ routing and multicast RPF
    - Supports IGMP v1/v2/v3 Snooping and MLD v1/v2 Snooping
    - Supports MVR
    - Supports DVMRP/PIM-DM/PIM-SM/MOSPF
    - Supports 4 Sets of 64-bit MIB counter
- Access Control List (ACL) Function
  - Supports 2K shared entry for VLAN and Ingress ACL
  - Supports L2/L3/L4 format and user defined field
  - Supports 256 policer for traffic policing DLB/srTCM/trTCM
  - Supports 2K 64-bit byte-based or packet-based log counters to enhance MIB counter
  - Supports action to Drop/Permit/Redirect/ Copy/Unicast Routing/Mirror/Logging/Policing/ Ingress VLAN conversion/Egress VLAN conversion/QoS remarking/VLAN tag status assignment
  - Range Check
    - VLAN
    - IPv4/IPv6 SIP/DIP
    - L4 SPORT/DPORT
    - Packet Length

- QoS Functions
  - 8 physical queues for normal port, 32 queues for internal CPU port
  - Priority Assignment based on IEEE 802.1P priority, DSCP value, physical port number, DMAC-based, SMAC-based, Ether-Type-based, CVID, SVID, IPv4 SIP, IPv4 DIP, IPv4/IPv6 TOS field, IPv6 Flow Label, TCP/UDP source/ destination port
  - Strict Priority (SP) and Weighted Fair Queue (WFQ), Weighted Round Robin (WRR) packet scheduling
  - Supports Fixed and Assured bandwidth control
  - QoS remarking for 802.1p and DSCP (includes IPv4/IPv6)
  - Supports average packet rate control leaky-bucket per queue, with 16Kbps steps from 16Kbps to 10Gbps
  - Supports ingress and egress port bandwidth control with 16Kbps steps from 16Kbps to 10Gbps
  - Simple Weighted Random Early Drop (SWRED) to prevent TCP Global Synchronization
  - Ethernet AV
    - IEEE 1588v2 supported by PHY
    - IEEE 802.1Qav
- Power Saving Function
  - Supports IEEE 802.3az EEE
- MIB Functions
  - MIB-II (RFC 1213)
  - Ethernet-like MIB (RFC 3635)
  - Interface Group MIB (RFC 2863)
  - RMON (RFC 2819)
  - Bridge MIB (RFC 1493)
  - Bridge MIB Extension (RFC 2674)
  - Private MIB Counter
- Others
  - 40nm CMOS process
  - 3.3V/1.1V power input
  - 1.5V for DDR3
  - EDHS-PBGA533 package

3. Block Diagram

3.1. Functional Block Diagram

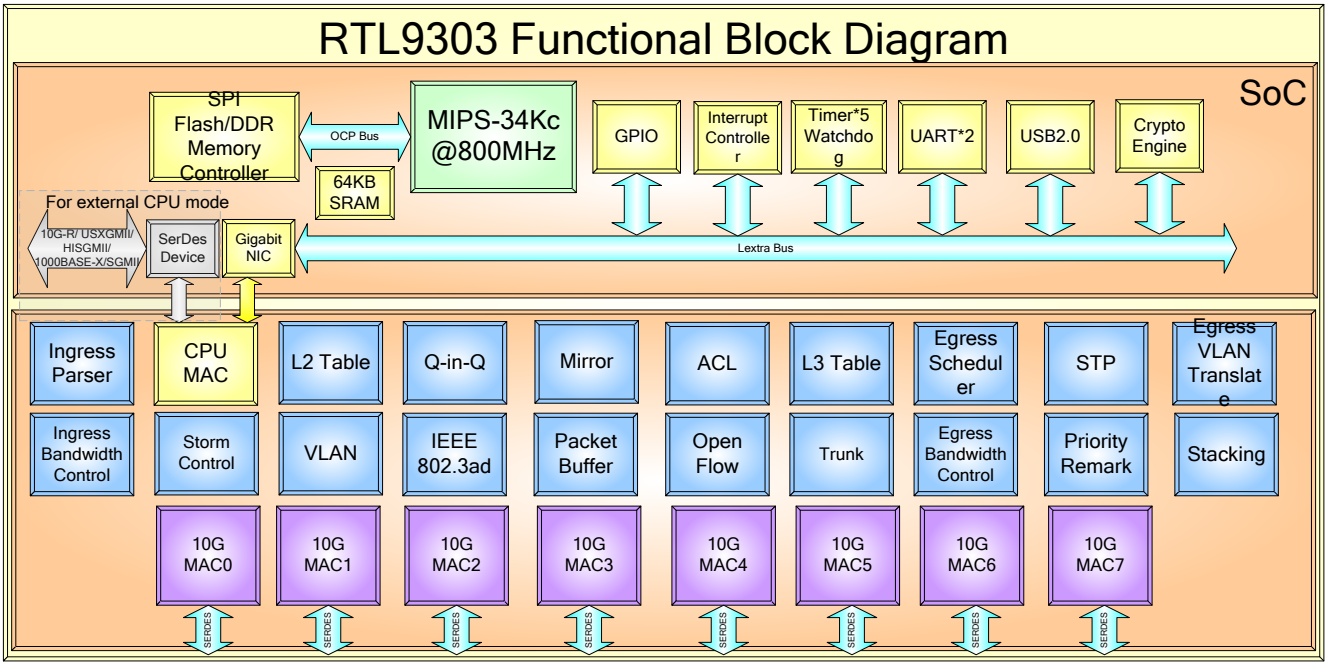


Figure 1. Functional Block Diagram

4. System Applications

*4.1. 8*10G Fiber*

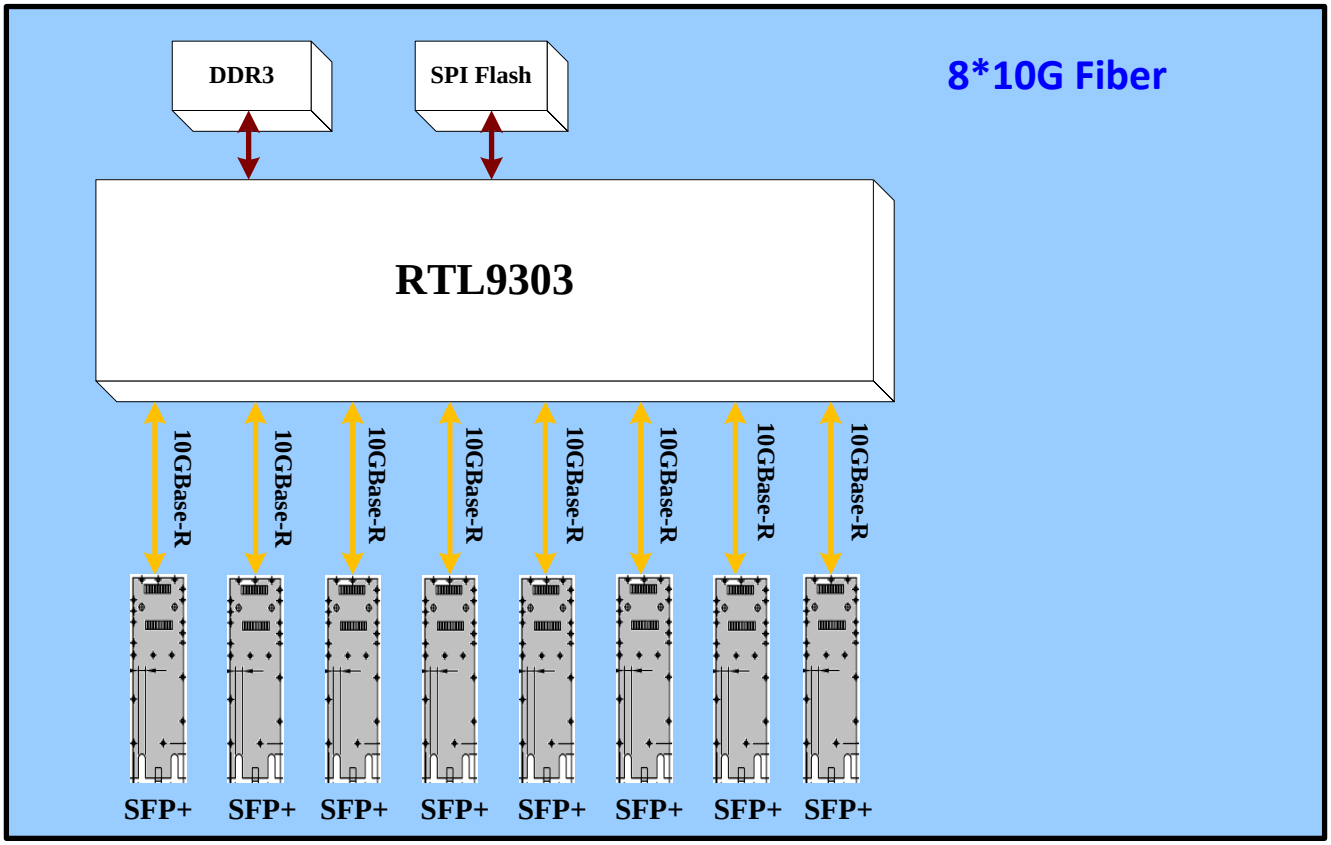


Figure 2. 8*10G Fiber

5. Pin Assignments

5.1. Pin Layout

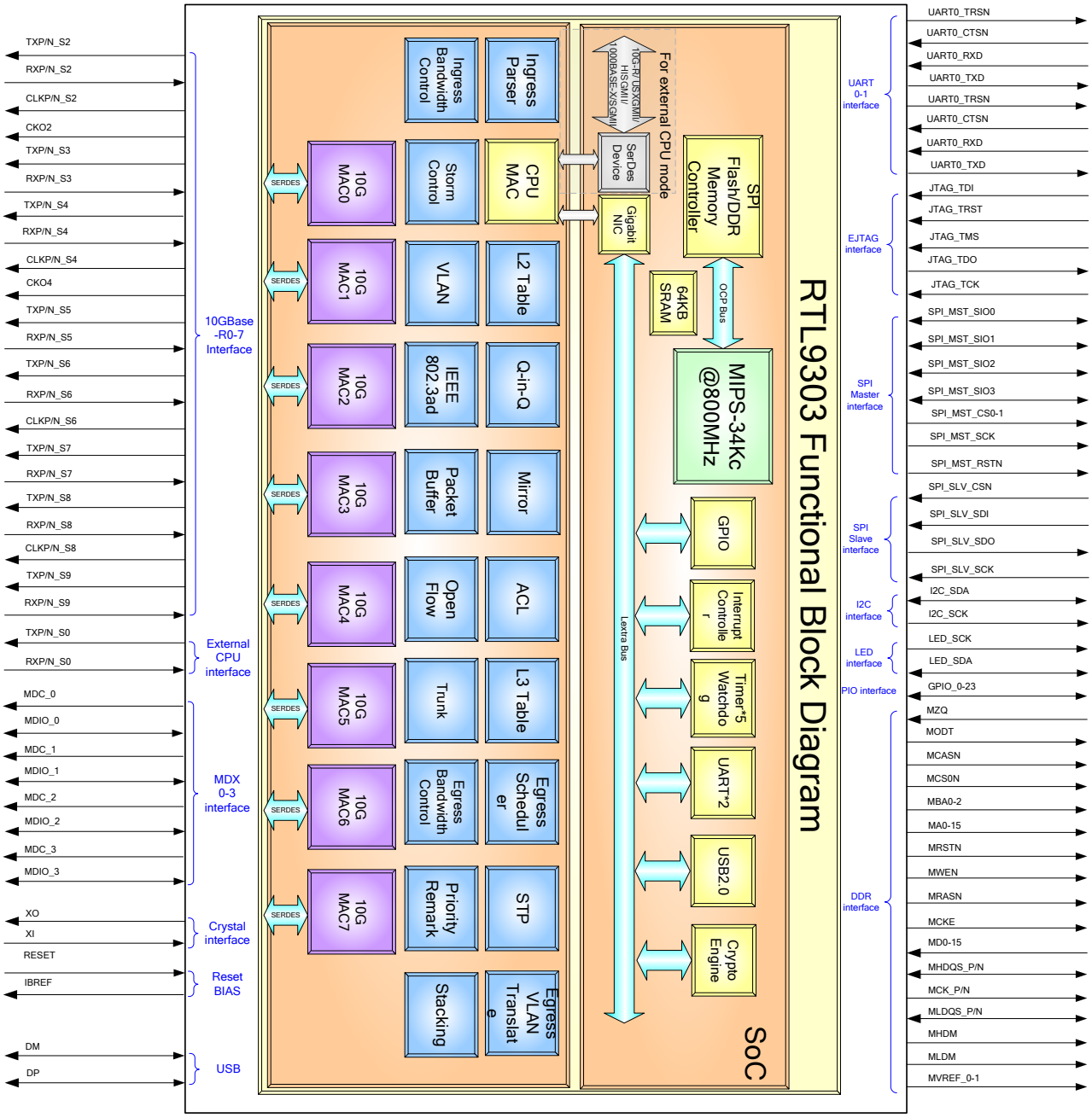


Figure 3. Pin Layout

5.2. Pin Assignments (Top View)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14
A	SLV_SPI_SDI	SLV_SPI_SCLK	SLV_SPI_SDO	JTAG_TDI	GPIO1	GPIO3	GPIO5	GPIO7	GPIO9	GPIO11	GPIO13	GPIO15	GPIO17	GPIO19
B	UART0_TXD	UART0_RXD	SLV_SPI_CS	JTAG_TMS	GPIO0	GPIO2	GPIO4	GPIO6	GPIO8	GPIO10	GPIO12	GPIO14	GPIO16	GPIO18
C	LED_MDC	LED_MDIO	UART0_RTS	JTAG_TRST	JTAG_TCK	EN_DECRYPT	BOOT_SEL	REG_IF_SEL	RST_CMD_DIS	GND	GND	GND	GND	GND
D	RESET	INT	RST_OUT	UART0_CTS	JTAG_TDO	RESERVED	CPU_SLEEP	MEM_TYPE	SYS_LED_EN	GND	GND	GND	GND	GND
E	SPI_MST_CS1	SPI_MST_CS0	GND	GND										
F	SPI_MST_SIO3	SPI_MST_SIO2	GND	DM										
G	SPI_MST_SIO1	SPI_MST_SIO0	GND	DP										
H	SPI_MST_SCK	SPI_MST_RSTN	GND	GND				DVDDL	DVDDL	GND	GND	GND	GND	GND
J	MZQ	MD4	GND	RREF					DVDDL	GND	GND	GND	GND	GND
K	MD6	MD2	GND	GND				DVDDL	DVDDL	GND	GND	GND	GND	GND
L	MD0	MHDM	AVDDH_USB	AVDDH_PLL2				DVDDL	DVDDL	GND	GND	GND	GND	GND
M	MD11	MD13	GND	GND					DVDDL	GND	GND	GND	GND	GND
N	MD15	MD9	AVDDL_USB	AVDDL_PLL2				DVDDL	DVDDL	GND	GND	GND	GND	GND
P	MLDQS	MLDQSN	GND	AVDDL_DLL				DVDDL	DVDDL	GND	GND	GND	GND	GND
R	MCKN	MCK	GND	GND					DVDDL	GND	GND	GND	GND	GND
T	MHDQS	MHDQSN	GND	GND				DVDDL	DVDDL	GND	GND	GND	GND	GND
U	MD12	MD14	GND	GND				DVDDL	DVDDL	GND	GND	GND	GND	GND
V	MD10	MD8	MVDDH	MVDDH				DVDDL	DVDDL	GND	GND	GND	GND	GND
W	MLDM	MD1	MVDDH	MVDDH					DVDDL	DVDDL	DVDDL	DVDDL	DVDDL	GND
Y	MD3	MD5	MVDDH	MVDDH				DVDDL	DVDDL	DVDDL	DVDDL	DVDDL	DVDDL	GND
AA	MD7	MCKE	MVREF0	MVREF1										
AB	MA10	BA1	GND	GND										
AC	MA4	MA6	GND	GND										
AD	MA8	MA11	GND	GND	GND	GND	AVDDL_PLL1	AVDDH_PLL1	DVDDH	SVDDH	SVDDH	PWRMON	AVDDH_CEN	AVDDH_XTAL
AE	MA14	MA1	GND	GND	GND	GND	GND	MA15	DVDDH	SVDDH	SVDDH	IBREF	GND	AVDDH_PLL0
AF	MA12	MWEN	MA0	MA13	MRSTN	MA5	BA0	MCASN	DVDDH	SVDDH	SVDDH	GND	XI	RESERVED
AG	MRASN	BA2	MA2	MA9	MA7	MA3	MCS0N	MODT	DVDDH	SVDDH	SVDDH	GND	XO	GND
	1	2	3	4	5	6	7	8	9	10	11	12	13	14

Figure 4. Pin Assignments (Top View)

15	16	17	18	19	20	21	22	23	24	25	26	27	
GPIO21	GPIO23	M3_MDC	SGND	HSIN_S9	SGND	HSON_S9	SGND	HSIP_S8	SGND	HSOP_S8	SGND	CLKP_S8	A
GPIO20	GPIO22	M3_MDIO	SGND	HSIP_S9	SGND	HSOP_S9	SGND	HSIN_S8	SGND	HSON_S8	SGND	CLKN_S8	B
GND	GND	DVDD_MDX3	GND	SGND	SGND	SGND	SGND	SGND	SGND	SGND	SGND	SGND	C
DVDDIO_G1	DVDDIO_G2	DVDDIO_G3	DVDDIO_G4	SGND	SGND	SGND	SGND	SGND	SGND	SGND	HSIP_S7	HSIN_S7	D
									SGND	SGND	SGND	SGND	E
									SGND	SGND	HSOP_S7	HSON_S7	F
									SGND	SGND	SGND	SGND	G
GND	GND	GND	SVDDL	SVDDL	SVDDL				SGND	SGND	HSIN_S6	HSIP_S6	H
GND	GND	GND	SVDDL	SVDDL	SVDDL				SGND	SGND	SGND	SGND	J
GND	GND	GND	GND	SGND	GNDCK3				SGND	SGND	HSON_S6	HSOP_S6	K
GND	GND	GND	GND	SGND	SGND				CLKN_S6	CLKP_S6	SGND	SGND	L
GND	GND	GND	GND	SGND	SGND				SGND	SGND	HSIP_S5	HSIN_S5	M
GND	GND	GND	GND	SGND	GNDCK2				AVDDL_CK	AVDDL_CK	SGND	SGND	N
GND	GND	GND	GND	SGND	SGND				SVDDL	SGND	HSOP_S5	HSON_S5	P
GND	GND	GND	GND	SGND	GNDCK1				SVDDL	SVDDL	SGND	SGND	R
GND	GND	GND	GND	SGND	SGND				SVDDL	SGND	HSIN_S4	HSIP_S4	T
GND	GND	GND	GND	SGND	GNDCK0				AVDDL_CK	AVDDL_CK	SGND	SGND	U
GND	GND	GND	GND	SVDDL	SVDDL				SGND	SGND	HSON_S4	HSOP_S4	V
GND	GND	GND	SVDDL	SVDDL	SVDDL				CLKN_S4	CLKP_S4	SGND	GND	W
GND	GND	GND	SVDDL	SVDDL	SVDDL				SGND	SGND	M2_MDIO	M2_MDC	Y
									SGND	CKO_4	SGND	SGND	AA
									SGND	SGND	HSIP_S3	HSIN_S3	AB
									CKO_2	SGND	SGND	SGND	AC
AVDDL_CEN	RTT2	AVDDL_PLL0	GND	DVDD_MDX0	DVDD_MDX1	DVDD_MDX2	CLKN_S2	M0_MDC	GND	SGND	HSOP_S3	HSON_S3	AD
RTT1	CKO_0	SGND	SGND	SGND	CKO_1	SGND	CLKP_S2	SGND	M0_MDIO	SGND	SGND	SGND	AE
HSON_S0	SGND	HSIN_S0	SGND	RESERVED	SGND	RESERVED	SGND	HSON_S2	SGND	HSIN_S2	SGND	M1_MDIO	AF
HSOP_S0	SGND	HSIP_S0	SGND	RESERVED	SGND	RESERVED	SGND	HSOP_S2	SGND	HSIP_S2	GND	M1_MDC	AG
15	16	17	18	19	20	21	22	23	24	25	26	27	

Figure 5. Pin Assignments (Top View) (Continued)

5.3. Pin Assignments Table Definitions

Upon Reset: Defined as a short time after the end of a hardware reset.

After Reset: Defined as the time after the specified 'Upon Reset' time.

I: Input Pin

O: Output Pin

I/O: Bi-Direction Input/Output Pin

DP: Digital Power Pin

DG: Digital Ground Pin

SP: SERDES Power Pin

MP: DDR Power Pin

AI: Analog Input Pin

AO: Analog Output Pin

AI/O: Analog Bi-Direction Input/Output Pin

AP: Analog Power Pin

AG: Analog Ground Pin

SG: SERDES Ground Pin

RP: Reference voltage for data for DDR SDRAM

I_{PU}: Input Pin With Pull-Up Resistor; (Typical Value = 75KΩ)

I_{PD}: Input Pin With Pull-Down Resistor; (Typical Value = 75KΩ)

O_{PU}: Output Pin With Pull-Up Resistor; (Typical Value = 75KΩ)

O_{PD}: Output Pin With Pull-Down Resistor; (Typical Value = 75KΩ)

5.4. Pin Assignments Table

Table 1. Pin Assignments Table

Pin Name	Pin No.	Type
SLV_SPI_SDI	A1	I/O_{PU}
SLV_SPI_SCLK	A2	I/O_{PU}
SLV_SPI_SDO	A3	I/O_{PD}
JTAG_TDI	A4	I/O_{PD}
GPIO1	A5	I/O_{PU}
GPIO3	A6	I/O_{PU}
GPIO5	A7	I/O_{PU}
GPIO7	A8	I/O_{PU}
GPIO9	A9	I/O_{PU}
GPIO11	A10	I/O_{PU}
GPIO13	A11	I/O_{PU}
GPIO15	A12	I/O_{PU}
GPIO17	A13	I/O_{PU}
GPIO19	A14	I/O_{PU}
GPIO21	A15	I/O_{PU}
GPIO23	A16	I/O_{PD}
M3_MDC	A17	O_{PU}
SGND	A18	SG
HSIN_S9	A19	AI
SGND	A20	SG
HSON_S9	A21	AO
SGND	A22	SG
HSIP_S8	A23	AI
SGND	A24	SG
HSOP_S8	A25	AO
SGND	A26	SG
CLKP_S8	A27	AO
UART0_TXD	B1	I/O_{PD}

Pin Name	Pin No.	Type
URAT0_RXD	B2	I_{PD}
SLV_SPI_CS	B3	I/O_{PU}
JTAG_TMS	B4	I/O_{PU}
GPIO0	B5	I/O_{PD}
GPIO2	B6	I/O_{PU}
GPIO4	B7	I/O_{PU}
GPIO6	B8	I/O_{PU}
GPIO8	B9	I/O_{PU}
GPIO10	B10	I/O_{PU}
GPIO12	B11	I/O_{PU}
GPIO14	B12	I/O_{PU}
GPIO16	B13	I/O_{PU}
GPIO18	B14	I/O_{PD}
GPIO20	B15	I/O_{PD}
GPIO22	B16	I/O_{PU}
M3_MDIO	B17	I/O_{PU}
SGND	B18	SG
HSIP_S9	B19	AI
SGND	B20	SG
HSOP_S9	B21	AO
SGND	B22	SG
HSIN_S8	B23	AI
SGND	B24	SG
HSON_S8	B25	AO
SGND	B26	SG
CLKN_S8	B27	AO
LED_MDC	C1	O_{PU}
LED_MDIO	C2	I/O_{PU}
UART0_RTS	C3	I/I_{PD}
JTAG_TRST	C4	I/O_{PD}
JTAG_TCK	C5	I/O_{PU}
EN_DECRYPT	C6	I_{PD}
BOOT_SEL	C7	I_{PD}
REG_IF_SEL	C8	I_{PD}
RST_CMD_DIS	C9	I_{PU}
GND	C10	DG
GND	C11	DG
GND	C12	DG
GND	C13	DG
GND	C14	DG
GND	C15	DG
GND	C16	DG
DVDD_MDX3	C17	DP
GND	C18	DG

Pin Name	Pin No.	Type
SGND	C19	SG
SGND	C20	SG
SGND	C21	SG
SGND	C22	SG
SGND	C23	SG
SGND	C24	SG
SGND	C25	SG
SGND	C26	SG
SGND	C27	SG
RESET	D1	AI
INT	D2	I/O_{PU}
RST_OUT	D3	O_{PU}
UART0_CTS	D4	I_{PU}
JTAG_TDO	D5	I/O_{PD}
RESERVED	D6	-
CPU_SLEEP	D7	I_{PD}
MEM_TYPE	D8	I_{PU}
SYS_LED_EN	D9	I_{PU}
GND	D10	DG
GND	D11	DG
GND	D12	DG
GND	D13	DG
GND	D14	DG
DVDDIO_G1	D15	DP
DVDDIO_G2	D16	DP
DVDDIO_G3	D17	DP
DVDDIO_G4	D18	DP
SGND	D19	SG
SGND	D20	SG
SGND	D21	SG
SGND	D22	SG
SGND	D23	SG
SGND	D24	SG
SGND	D25	SG
HSIP_S7	D26	AI
HSIN_S7	D27	AI
SPI_MST_CS1	E1	O_{PU}
SPI_MST_CS0	E2	O_{PU}
GND	E3	DG
GND	E4	DG
SGND	E24	SG
SGND	E25	SG
SGND	E26	SG
SGND	E27	SG

Pin Name	Pin No.	Type
SPI_MST_SIO3	F1	I/O_{PU}
SPI_MST_SIO2	F2	I/O_{PU}
GND	F3	DG
DM	F4	AIO
SGND	F24	SG
SGND	F25	SG
HSOP_S7	F26	AO
HSON_S7	F27	AO
SPI_MST_SIO1	G1	I/O_{PU}
SPI_MST_SIO0	G2	I/O_{PU}
GND	G3	DG
DP	G4	AIO
SGND	G24	SG
SGND	G25	SG
SGND	G26	SG
SGND	G27	SG
SPI_MST_SCK	H1	O_{PD}
SPI_MST_RSTN	H2	O_{UP}
GND	H3	DG
GND	H4	DG
DVDDL	H8	DP
DVDDL	H9	DP
GND	H10	DG
GND	H11	DG
GND	H12	DG
GND	H13	DG
GND	H14	DG
GND	H15	DG
GND	H16	DG
GND	H17	DG
SVDDL	H18	SP
SVDDL	H19	SP
SVDDL	H20	SP
SGND	H24	SG
SGND	H25	SG
HSIN_S6	H26	AI
HSIP_S6	H27	AI
MZQ	J1	I
MD4	J2	I/O
GND	J3	DG
RREF	J4	RP
DVDDL	J9	DP
GND	J10	DG
GND	J11	DG

Pin Name	Pin No.	Type
GND	J12	DG
GND	J13	DG
GND	J14	DG
GND	J15	DG
GND	J16	DG
GND	J17	DG
SVDDL	J18	SP
SVDDL	J19	SP
SVDDL	J20	SP
SGND	J24	SG
SGND	J25	SG
SGND	J26	SG
SGND	J27	SG
MD6	K1	I/O
MD2	K2	I/O
GND	K3	DG
GND	K4	DG
DVDDL	K8	DP
DVDDL	K9	DP
GND	K10	DG
GND	K11	DG
GND	K12	DG
GND	K13	DG
GND	K14	DG
GND	K15	DG
GND	K16	DG
GND	K17	DG
GND	K18	DG
SGND	K19	SG
GNDCK3	K20	AG
SGND	K24	SG
SGND	K25	SG
HSON_S6	K26	AI
HSOP_S6	K27	AI
MD0	L1	I/O
MHDM	L2	O
AVDDH_USB	L3	AP
AVDDH_PLL2	L4	AP
DVDDL	L8	DP
DVDDL	L9	DP
GND	L10	DG
GND	L11	DG
GND	L12	DG
GND	L13	DG

Pin Name	Pin No.	Type
GND	L14	DG
GND	L15	DG
GND	L16	DG
GND	L17	DG
GND	L18	DG
SGND	L19	SG
SGND	L20	SG
CLKN_S6	L24	AO
CLKP_S6	L25	AO
SGND	L26	SG
SGND	L27	SG
MD11	M1	I/O
MD13	M2	I/O
GND	M3	DG
GND	M4	DG
DVDDL	M9	DP
GND	M10	DG
GND	M11	DG
GND	M12	DG
GND	M13	DG
GND	M14	DG
GND	M15	DG
GND	M16	DG
GND	M17	DG
GND	M18	DG
SGND	M19	SG
SGND	M20	SG
SGND	M24	SG
SGND	M25	SG
HSIP_S5	M26	AI
HSIN_S5	M27	AI
MD15	N1	I/O
MD9	N2	I/O
AVDDL_USB	N3	AP
AVDDL_PLL2	N4	AP
DVDDL	N8	DP
DVDDL	N9	DP
GND	N10	DG
GND	N11	DG
GND	N12	DG
GND	N13	DG
GND	N14	DG
GND	N15	DG
GND	N16	DG

Pin Name	Pin No.	Type
GND	N17	DG
GND	N18	DG
SGND	N19	SG
GNDCK2	N20	AG
AVDDL_CK	N24	AP
AVDDL_CK	N25	AP
SGND	N26	SG
SGND	N27	SG
MLDQS	P1	I/O
MLDQSN	P2	I/O
GND	P3	DG
AVDDL_DLL	P4	AP
DVDDL	P8	DP
DVDDL	P9	DP
GND	P10	DG
GND	P11	DG
GND	P12	DG
GND	P13	DG
GND	P14	DG
GND	P15	DG
GND	P16	DG
GND	P17	DG
GND	P18	DG
SGND	P19	SG
SGND	P20	SG
SVDDL	P24	SP
SGND	P25	SG
HSOP_S5	P26	AO
HSON_S5	P27	AO
MCKN	R1	I/O
MCK	R2	I/O
GND	R3	DG
GND	R4	DG
DVDDL	R9	DP
GND	R10	DG
GND	R11	DG
GND	R12	DG
GND	R13	DG
GND	R14	DG
GND	R15	DG
GND	R16	DG
GND	R17	DG
GND	R18	DG
SGND	R19	SG

Pin Name	Pin No.	Type
GNDCK1	R20	AG
SVDDL	R24	SP
SVDDL	R25	SP
SGND	R26	SG
SGND	R27	SG
MHDQS	T1	I/O
MHDQSN	T2	I/O
GND	T3	DG
GND	T4	DG
DVDDL	T8	DP
DVDDL	T9	DP
GND	T10	DG
GND	T11	DG
GND	T12	DG
GND	T13	DG
GND	T14	DG
GND	T15	DG
GND	T16	DG
GND	T17	DG
GND	T18	DG
SGND	T19	SG
SGND	T20	SG
SVDDL	T24	SP
SGND	T25	SG
HSIN_S4	T26	AI
HSIP_S4	T27	AI
MD12	U1	I/O
MD14	U2	I/O
GND	U3	DG
GND	U4	DG
DVDDL	U8	DP
DVDDL	U9	DP
GND	U10	DG
GND	U11	DG
GND	U12	DG
GND	U13	DG
GND	U14	DG
GND	U15	DG
GND	U16	DG
GND	U17	DG
GND	U18	DG
SGND	U19	SG
GNDCK0	U20	AG
AVDDL_CK	U24	AP

Pin Name	Pin No.	Type
AVDDL_CK	U25	AP
SGND	U26	SG
SGND	U27	SG
MD10	V1	I/O
MD8	V2	I/O
MVDDH	V3	MP
MVDDH	V4	MP
DVDDL	V8	DP
DVDDL	V9	DP
GND	V10	DG
GND	V11	DG
GND	V12	DG
GND	V13	DG
GND	V14	DG
GND	V15	DG
GND	V16	DG
GND	V17	DG
GND	V18	DG
SVDDL	V19	SP
SVDDL	V20	SP
SGND	V24	SG
SGND	V25	SG
HSON_S4	V26	AO
HSOP_S4	V27	AO
MLDM	W1	O
MD1	W2	I/O
MVDDH	W3	MP
MVDDH	W4	MP
DVDDL	W9	DP
DVDDL	W10	DP
DVDDL	W11	DP
DVDDL	W12	DP
DVDDL	W13	DP
GND	W14	DG
GND	W15	DG
GND	W16	DG
GND	W17	DG
SVDDL	W18	SP
SVDDL	W19	SP
SVDDL	W20	SP
CLKN_S4	W24	AO
CLKP_S4	W25	AO
SGND	W26	SG
GND	W27	DG

Pin Name	Pin No.	Type
MD3	Y1	I/O
MD5	Y2	I/O
MVDDH	Y3	MP
MVDDH	Y4	MP
DVDDL	Y8	DP
DVDDL	Y9	DP
DVDDL	Y10	DP
DVDDL	Y11	DP
DVDDL	Y12	DP
DVDDL	Y13	DP
GND	Y14	DG
GND	Y15	DG
GND	Y16	DG
GND	Y17	DG
SVDDL	Y18	SP
SVDDL	Y19	SP
SVDDL	Y20	SP
SGND	Y24	SG
SGND	Y25	SG
M2_MDIO	Y26	I/O_{PU}
M2_MDC	Y27	O_{PU}
MD7	AA1	I/O
MCKE	AA2	O
MVREF0	AA3	RP
MVREF1	AA4	RP
SGND	AA24	SG
CKO4	AA25	AO
SGND	AA26	SG
SGND	AA27	SG
MA10	AB1	O
BA1	AB2	O
GND	AB3	DG
GND	AB4	DG
SGND	AB24	SG
SGND	AB25	SG
HSIP_S3	AB26	AI
HSIN_S3	AB27	AI
MA4	AC1	O
MA6	AC2	O
GND	AC3	DG
GND	AC4	DG
CKO2	AC24	AO
SGND	AC25	SG
SGND	AC26	SG

Pin Name	Pin No.	Type
SGND	AC27	SG
MA8	AD1	O
MA11	AD2	O
GND	AD3	DG
GND	AD4	DG
GND	AD5	DG
GND	AD6	DG
AVDDL_PLL1	AD7	AP
AVDDH_PLL1	AD8	AP
DVDDH	AD9	DP
SVDDH	AD10	SP
SVDDH	AD11	SP
PWRMON	AD12	AI
AVDDH_CEN	AD13	AP
AVDDH_XTAL	AD14	AP
AVDDL_CEN	AD15	AP
RTT2	AD16	AI/O
AVDDL_PLL0	AD17	AP
GND	AD18	DG
DVDD_MDX0	AD19	DP
DVDD_MDX1	AD20	DP
DVDD_MDX2	AD21	DP
CLKN_S2	AD22	AO
M0_MDC	AD23	O_{PU}
GND	AD24	DG
SGND	AD25	SG
HSOP_S3	AD26	AO
HSON_S3	AD27	AO
MA14	AE1	O
MA1	AE2	O
GND	AE3	DG
GND	AE4	DG
GND	AE5	DG
GND	AE6	DG
GND	AE7	DG
MA15	AE8	O
DVDDH	AE9	DP
SVDDH	AE10	SP
SVDDH	AE11	SP
IBREF	AE12	AI/O
GND	AE13	DG
AVDDH_PLL0	AE14	AP
RTT1	AE15	AI/O
CKO0	AE16	AO

Pin Name	Pin No.	Type
SGND	AE17	SG
SGND	AE18	SG
SGND	AE19	SG
CKO1	AE20	AO
SGND	AE21	SG
CLKP_S2	AE22	AO
SGND	AE23	SG
M0_MDIO	AE24	I/O_{PU}
SGND	AE25	SG
SGND	AE26	SG
SGND	AE27	SG
MA12	AF1	O
MWEN	AF2	O
MA0	AF3	O
MA13	AF4	O
MRSTN	AF5	O
MA5	AF6	O
BA0	AF7	O
MCASN	AF8	O
DVDDH	AF9	DP
SVDDH	AF10	SP
SVDDH	AF11	SP
GND	AF12	DG
XI	AF13	AI
RESERVED	AF14	-
HSON_S0	AF15	AO
SGND	AF16	SG
HSIN_S0	AF17	AI
SGND	AF18	SG
RESERVED	AF19	-
SGND	AF20	SG
RESERVED	AF21	-
SGND	AF22	SG

Pin Name	Pin No.	Type
HSON_S2	AF23	AO
SGND	AF24	SG
SHIN_S2	AF25	AI
SGND	AF26	SG
M1_MDIO	AF27	I/O_{PU}
MRASN	AG1	O
BA2	AG2	O
MA2	AG3	O
MA9	AG4	O
MA7	AG5	O
MA3	AG6	O
MCS0N	AG7	O
MODT	AG8	O
DVDDH	AG9	DP
SVDDH	AG10	SP
SVDDH	AG11	SP
GND	AG12	DG
XO	AG13	AO
GND	AG14	DG
HSOP_S0	AG15	AO
SGND	AG16	SG
HSIP_S0	AG17	AI
SGND	AG18	SG
RESERVED	AG19	-
SGND	AG20	SG
RESERVED	AG21	-
SGND	AG22	SG
HSOP_S2	AG23	AO
SGND	AG24	SG
HSIP_S2	AG25	AI
GND	AG26	DG
M1_MDC	AG27	O_{PU}

6. Pin Descriptions

6.1. DDR3 SDRAM Interface

Table 2. DDR3 SDRAM Interface Pins

Pin Name	Pin No.	Type	Description
MD[15:0]	N1,U2,M2,U1,M1,V1,N2,V2,AA1,K1,Y2,J2,Y1,K2,W2,L1	I/O	Data Input/Output: Bi-directional data bus.
MA[15:0]	AE8,AE1,AF4,AF1,AD2,AB1,AG4,AD1,AG5,AC2,AF6,AC1,AG6,AG3,AE2,AF3	O	Address Outputs.
BA[2:0]	AG2,AB2,AF7	O	Bank Address Outputs.
MLDM	W1	O	Data Masks for lower-byte.
MHDM	L2	O	Data Masks for upper-byte.
MRASN MCASN MWEN	AG1 AF8 AF2	O	Command Outputs: MRASN, MCASN, MWEN (along with MCSN) define the command being entered.
MCS0N	AG7	O	Chip Select: MCSN enables (registered LOW) and disables (registered HIGH) the command decoder. All commands are masked when CS# is registered HIGH.
MCK_P MCK_N	R2 R1	O	Clock: MCK_P and MCK_N are differential clock outputs.
MCKE	AA2	O	Clock Enable: MCKE HIGK activates.
MLDQS_P MLDQS_N	P1 P2	I/O	Lower byte data strobe.
MHDQS_P MHDQS_N	T1 T2	I/O	Upper byte data strobe.
MRSTN	AF5	O	Active Low Reset.
MODT	AG8	O	On Die Termination: ODT (registered HIGH) enables termination resistance internal to the DDR3 SDRAM.
MZQ	J1	I	External reference ball for output drive calibration.

6.2. UART Interface

Table 3. UART Interface Pins

Pin Name	Pin No.	Type	Description
UART0_TXD	B1	I/O	UART0 Interface Transmit Data.
UART0_RXD	B2	I	UART0 Interface Receive Data.
UART0_RTS	C3	I/O	UART0 Interface Request to Send.
UART0_CTS	D4	I	UART0 Interface Clear to Send.
UART1_TXD	D5	I/O	UART1 Interface Transmit Data.
UART1_RXD	A4	I/O	UART1 Interface Receive Data.
UART1_RTS	B4	I/O	UART1 Interface Request to Send.
UART1_CTS	C5	I/O	UART1 Interface Clear to Send.

6.3. EJTAG Interface

Table 4. EJTAG Interface Pins

Pin Name	Pin No.	Type	Description
JTAG_TMS	B4	I/O	JTAG Test Mode Select.
JTAG_TCK	C5	I/O	JTAG Test Clock Input.
JTAG_TRST	C4	I/O	JTAG Test Reset.
JTAG_TDI	A4	I/O	JTAG Test Data Input..
JTAG_TDO	D5	I/O	JTAG Test Data Output.

6.4. GPIO Interface

Table 5. GPIO Interface Pins

Pin Name	Pin No.	Type	Description
GPIO[23:0]	A16,B16,A15,B15,A14,B14,A13, B13,A12,B12,A11,B11,A10,B10,A9, B9,A8,B8,A7,B7,A6,B6,A5,B5	I/O	General Purpose Input/Output. Provides configurable I/O ports that can be configured for either input or output.

6.5. SGMII Interface

Table 6. SGMII Interface Pins

Pin Name	Pin No.	Type	Description
HSOP_S0/ HSON_S0	AG15 AF15	AO	SGMII (1.25G) Transmit Data Differential Output Pair (For external CPU)
HSIP_S0/ HSIN_S0	AG17 AF17	AI	SGMII (1.25G) Receive Data Differential Input Pair (For external CPU) These pins must be pulled low with a 1K resistor when not used.

6.6. 10GBase-R Interface

Table 7. 10GBase-R Interface Pins

Pin Name	Pin No.	Type	Description
HSOP_S2/ HSON_S2	AG23 AF23	AO	10GBase-R (10.3125G) Transmit Data Differential Output Pair.
HSIP_S2/ HSIN_S2	AG25 AF25	AI	10GBase-R (10.3125G) Receive Data Differential Input Pair. These pins must be pulled low with a 1K resistor when not used.
HSOP_S3/ HSON_S3	AD26 AD27	AO	10GBase-R (10.3125G) Transmit Data Differential Output Pair.
HSIP_S3/ HSIN_S3	AB26 AB27	AI	10GBase-R (10.3125G) Receive Data Differential Input Pair. These pins must be pulled low with a 1K resistor when not used.
HSOP_S4/ HSON_S4	V27 V26	AO	10GBase-R (10.3125G) Transmit Data Differential Output Pair.
HSIP_S4/ HSIN_S4	T27 T26	AI	10GBase-R (10.3125G) Receive Data Differential Input Pair. These pins must be pulled low with a 1K resistor when not used.
HSOP_S5/ HSON_S5	P26 P27	AO	10GBase-R (10.3125G) Transmit Data Differential Output Pair.
HSIP_S5/ HSIN_S5	M26 M27	AI	10GBase-R (10.3125G) Receive Data Differential Input Pair. These pins must be pulled low with a 1K resistor when not used.
HSOP_S6/ HSON_S6	K27 K26	AO	10GBase-R (10.3125G) Transmit Data Differential Output Pair.
HSIP_S6/ HSIN_S6	H27 H26	AI	10GBase-R (10.3125G) Receive Data Differential Input Pair. These pins must be pulled low with a 1K resistor when not used.
HSOP_S7/ HSON_S7	F26 F27	AO	10GBase-R (10.3125G) Transmit Data Differential Output Pair.
HSIP_S7/ HSIN_S7	D26 D27	AI	10GBase-R (10.3125G) Receive Data Differential Input Pair. These pins must be pulled low with a 1K resistor when not used.
HSOP_S8/ HSON_S8	A25 B25	AO	10GBase-R (10.3125G) Transmit Data Differential Output Pair.
HSIP_S8/ HSIN_S8	A23 B23	AI	10GBase-R (10.3125G) Receive Data Differential Input Pair. These pins must be pulled low with a 1K resistor when not used.
HSOP_S9/ HSON_S9	B21 A21	AO	10GBase-R (10.3125G) Transmit Data Differential Output Pair.

Pin Name	Pin No.	Type	Description
HSIP_S9/ HSIN_S9	B19 A19	AI	10GBase-R (10.3125G) Receive Data Differential Input Pair. These pins must be pulled low with a 1K resistor when not used.

6.7. LED Interface

Table 8. LED Interface Pins

Pin Name	Pin No.	Type	Description
LED_MDC	C1	O	Controller Clock for LED.
LED_MDIO	C2	I/O	Controller Data for LED.
SYS_LED	B5	I/O	System LED.

6.8. SPI Master Interface

Table 9. SPI Master Interface Pins

Pin Name	Pin No.	Type	Description
SPI_MST_CS[1:0]	E1,E2	O	Chip select 1-0.
SPI_MST_SCK	H1	O	Clock output.
SPI_MST_RSTN	H2	O	Chip reset.
SPI_MST_SIO0	G2	I/O	Serial data output (for 1Xi/O)/ Serial data input & output (for 2Xi/O or 4Xi/O).
SPI_MST_SIO1	G1	I/O	Serial data input (for 1Xi/O)/ Serial data input & output (for 2Xi/O or 4Xi/O).
SPI_MST_SIO2	F2	I/O	Serial data input & output (for 4Xi/O).
SPI_MST_SIO3	F1	I/O	Serial data input & output (for 4Xi/O).

6.9. SPI Slave Interface

Table 10. SPI Slave Interface Pins

Pin Name	Pin No.	Type	Description
SPI_SLV_CS	B3	I	Chip select.
SPI_SLV_SCLK	A2	I	Clock input.
SPI_SLV_SDI	A1	I	Serial data input.
SPI_SLV_SDO	A3	O	Serial data output.

6.10. USB Interface

Table 11. USB Interface Pins

Pin Name	Pin No.	Type	Description
DM DP	F4 G4	AI/O	USB Date Differential input/output Pair.
RREF	J4	RP	Reference Resistor for BG. A 12KΩ (1%) resistor should be connected between RREF and GND.

6.11. Miscellaneous Interface

Table 12. Miscellaneous Interface Pins

Pin Name	Pin No.	Type	Description
M0_MDC	AD23	O	MII 0 Management Interface Clock Pin.
M0_MDIO	AE24	I/O	MII 0 Management Interface Data Pin.
M1_MDC	AG27	O	MII 1 Management Interface Clock Pin.
M1_MDIO	AF27	I/O	MII 1 Management Interface Data Pin.
M2_MDC	Y27	O	MII 2 Management Interface Clock Pin.
M2_MDIO	Y26	I/O	MII 2 Management Interface Data Pin.
M3_MDC	A17	O	MII 3Management Interface Clock Pin.
M3_MDIO	B17	I/O	MII 3 Management Interface Data Pin.
XI	AF13	AI	25MHz Crystal Clock Input Pin.
XO	AG13	AO	25MHz Crystal Clock Output Pin.
RESET	D1	AI	System Reset Input Pin.
RST_OUT	D3	O	Reset signal output
IBREF	AE12	AI/O	Reference Resistor for BG. A 2.49KΩ (1%) resistor should be connected between IBREF and GND.
PWRMON	AD12	AI	For power monitor use.
INT	D2	I/O	Interrupt signal output.
CKO0/1/2/4	AE16,AE20,AC24,AA25	AO	25MHz clock output.
CLKP_S8/6/4/2 CLKN_S8/6/4/2	A27,L25,W25,AE22 B27,L24,W24,AD22	AO	SERDES Differential clock Output Pair.
RTT1 RTT2	AE15 AD16	AI/O	Reserved for internal Use (Must be left floating)
RESERVED	AF14, D6,AF19,AF21,AG19,AG21	-	Reserved for internal Use

6.12. Configuration (Pin Strapping Function)

Table 13. Configuration Strapping Pins

Pin Name	Pin No.	Default	Description
EN_DECRYPT	C6	0b0	Enable or disable decrypt for flash. 0b0: Disable decrypt. 0b1: Enable decrypt
CPU_SLEEP	D7	0b0	Selection CPU station. 0b0: CPU is in normal state 0b1: CPU is always under reset state
BOOT_SEL	C7	0b0	Boot up flash selection. 0b0: SPI NOR flash 1b1: ROM Definition of SYNC MCR[27:24]. Report the hardware strapping initial value for boot flash type. 0b0000: SPI-NOR Flash 0b0010: ROM Boot Others: Reserved
MEM_TYPE	D8	0b1	DDR_TYPE(SYNC MCR[31:28]). 0b0: DDR2 0b1: DDR3 Note: no DDR mode should be set by S/W. Definition of SYNC MCR[31:28]. Report the hardware strapping initial value for DRAM type. 0b0001: DDR2 0b0010: DDR3 Others: Reserved
SYS_LED_EN	D9	0b1	Enable system LED. 0b0: Disable 0b1: Enable Note: When enable system LED, the GPIO[0] change to system LED pin.
REG_IF_SEL	C8	0b0	Select Register Access Interface. 0b0: Register can only be accessed by EEPROM SMI Slave interface 0b1: Register can only be accessed by SPI Slave interface
RST_CMD_DIS	C9	0b1	Indicates whether issuing 0x66,0x99 SPI flash commands or not when before booting from SPI flash. 0b0: Issue 0x66,0x99 SPI flash commands 0b1: Issue no reset commands

6.13. Power and GND

Table 14. Power and GND Pins

Pin Name	Pin No.	Type	Description
SVDDH	AD10, AD11, AE10, AE11, AF10, AF11, AG10, AG11	SP	SERDES High Voltage Power.
SVDDL	H18, H19, H20, J18, J19, J20, P24, R24, R25, T24, V19, V20, W18, W19, W20, Y18, Y19, Y20	SP	SERDES Low Voltage Power.
DVDDH	AD9, AE9, AF9, AG9	DP	Digital High Voltage Power.
DVDDL	H8, H9, J9, K8, K9, L8, L9, M9, N8, N9, P8, P9, R9, T8, T9, U8, U9, V8, V9, W9, W10, W11, W12, W13, Y8, Y9, Y10, Y11, Y12, Y13	DP	Digital Low Voltage Power.
DVDDIO_G4/3/2/1	D18, D17, D16, D15	DP	Digital Power for GPIO pins.
DVDD_MDX3/2/1/0	C17, AD21, AD20, AD19	DP	Digital Power for MDX circuit.
AVDDH_USB	L3	AP	USB High Voltage Power.
AVDDL_USB	N3	AP	USB Low Voltage Power.
AVDDL_DLL	P4	AP	DLL Low Voltage Power.
AVDDL_CK	N24, N25, U24, U25	AP	CMU Low Voltage Power..
AVDDH_PLL2/1/0	L4, AD8, AE14	AP	PLL High Voltage Power.
AVDDL_PLL2/1/0	N4, AD7, AD17	AP	PLL Low Voltage Power.
AVDDH_CEN	AD13	AP	Central Port High Voltage Power
AVDDL_CEN	AD15	AP	Central Port Low Voltage Power
AVDDH_XTAL	AD14	AP	XTAL High Voltage Power
MVDDH	V3, V4, W3, W4, Y3, Y4	MP	Power for DDR SDRAM.
MVREF1/0	AA4, AA3	RP	Reference voltage for data for DDR SDRAM.

Pin Name	Pin No.	Type	Description
GND	C10, C11.C12, C13, C14, C15, C16, C18, D10, D11, D12, D13, D14, E3, E4, F3, G3, H3, H4, H10, H11, H12, H13, H14, H15, H16, H17, J3, J10, J11, J12, J13, J14, J15, J16, J17, K3, K4, K10, K11, K12, K13, K14, K15, K16, K17, K18, L10, L11, L12, L13, L14, L15, L16, L17, L18, M3, M4, M10, M11, M12, M13, M14, M15, M16, M17, M18, N10, N11, N12, N13, N14, N15, N16, N17, N18, P3, P10, P11, P12, P13, P14, P15, P16, P17, P18, R3, R4, R10, R11, R12, R13, R14, R15, R16, R17, R18, T3, T4, T10, T11, T12, T13, T14, T15, T16, T17, T18, U3, U4, U10, U11, U12, U13, U14, U15, U16, U17, U18, V10, V11, V12, V13, V14, V15, V16, V17, V18, W14, W15, W16, W17, W27, Y14, Y15, Y16, Y17, AB3, AB4, AC3, AC4, AD3, AD4, AD5, AD6, AD18, AD24, AE3, AE4, AE5, AE6, AE7, AE13, AF12, AG12, AG14, AG26	DG	Digital Ground.
SGND	A18, A20, A22, A24, A26, B18, B20, B22, B24, B26, C19, C20, C21, C22, C23, C24, C25, C26, C27, D19, D20, D21, D22, D23, D24, D25, E24, E25, E26, E27, F24, F25, G24, G25, G26, G27, H24, H25, J24, J25, J26, J27, K19, K24, K25, L19, L20, L26, L27, M19, M20, M24, M25, N19, N26, N27, P19, P20, P25, R19, R26, R27, T19, T20, T25, U19, U26, U27, V24, V25, W26, Y24, Y25, AA24, AA26, AA27, AB24, AB25, AC25, AC26, AC27, AD25, AE17, AE18, AE19, AE21, AE23, AE25, AE26, AE27, AF16, AF18, AF20, AF22, AF24, AF26, AG16, AG18, AG20, AG22, AG24	SG	SERDES Ground.
GNDCK3/2/1/0	K20, N20, R20, U20	G	Ground for CMU.

7. Switch Function Description

7.1. Hardware Reset and Software Reset

7.1.1. Hardware Reset

A hardware reset forces the RTL9303 to start the initial power-on sequence. The hardware will strap pins to give all default values when the 'RESET' signal terminates. Next the configuration is cleared to chip default, and then the complete SRAM BIST (Built-In Self-Test) process is run. Finally the packet buffer descriptors are initialized and internal registers can be accessed by the internal/external CPU.

7.1.2. Software Reset

The RTL9303 supports three software resets, CPU & Memory reset, Switch NIC reset, and Software Switch reset. Reset sources are the signals that will trigger the reset command to the chip. All reset signals are low active.

- CPU & Memory reset: Resets MIPS 34Kc + Memory Controller + Peripheral + LXB + NIC
- Switch NIC reset: Resets NIC interface between CPU and Switch
- Switch Soft reset: Resets whole switch core

7.2. Layer 2 Learning and Forwarding

The RTL9303 has a 4K-entry VLAN table which is used by 802.1Q and Q-in-Q VLAN. IVL (Individual VLAN Learning), SVL (Shared VLAN learning) and IVL/SVL mixed mode are supported and per VLAN basis can specify the VLAN learning mode for unicast/broadcast and L2/IP multicast traffic respectively.

7.2.1. Forwarding

L2 multicast data packets involve L2 and multicast group table lookup. If the L2 table lookup returns a hit, the data packet is forwarded to all member ports and router ports retrieved from multicast group table. If the multicast address is not stored in the address table (i.e., lookup miss), the packet is broadcast to all ports of the broadcast domain. The VLAN Frame Forwarding Rules are defined as follows:

The received unknown unicast/unknown multicast/broadcast frame will be flooded to VLAN member ports and the source port is excluded.

The received unicast frame will be forwarded to its destination port only if the destination port is in the same VLAN as the source port. If the destination port belongs to a different VLAN, the frame will be discarded.

7.2.2. Learning

The RTL9303 supports a 16K-entry Layer 2 table. It uses a 2-left 4-way hash structure to store L2 entries. Each entry can be recorded in two formats; L2 Unicast and L2 Multicast. Layer 3 IP Multicast traffic Layer 3 tables are downgraded to L2 Multicast. The L2 Unicast and Multicast hash key is (FID/VID, MAC).

The learnt unicast entries are aged out after the specified aging period. The RTL9303 per port supports a configuration to disable the aging out function.

7.3. Layer 2 Learning Constraint

The RTL9303 supports system-based, port-based, trunk-based, and VLAN-based layer 2 learning constraint. The function is to limit the number of learnt MAC addresses on the system, particularly port, trunk, and VLAN.

For system-based learning constraint, there is a configuration for users to define the MAC address numbers that the system can learn. For port-based learning constraint, each port has a configuration to define the MAC address number that the port can learn. For trunk-based learning constraint, each trunk has a configuration to define the MAC address number that the trunk can learn. For VLAN-based learning constraint, there are 8 configurations supported to define the MAC address number that the particular VLAN can learn.

The packets are dropped, forwarded, or trapped to the CPU when the learnt L2 entries number reaches the limited number. Three learning constraint functions can work simultaneously and the action priority is Drop > Trap > Copy > Forward if the learning constraint actions are triggered at the same time.

7.4. Port Isolation

Port Isolation function is used to control whether the hosts can communicate with each other or not.

If we set the register to cut the connection between hosts, all packets from a host (downlink port) cannot be transmitted to another host directly. These packets can only be transmitted by passing through the router (uplink port) as illustrated below.

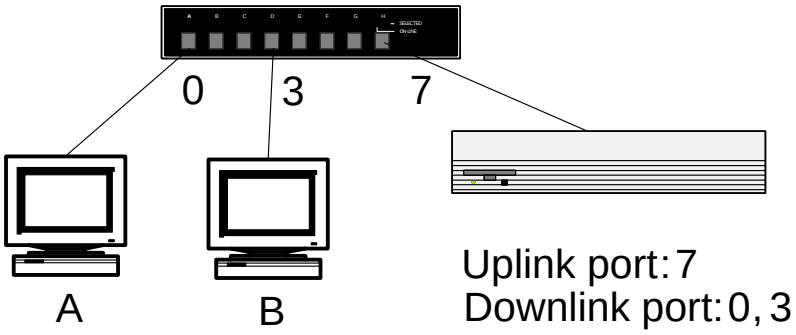


Figure 6. Port Isolation Example

Port-based port isolation is archived by providing a port mask configuration for each ingress port. The port mask is used to indicate the ports that allow forwarding of traffic.

The Mirroring function is not limited by the port isolation port mask, that is, the mirroring port does not have to be within the port mask.

In addition to port-based port isolation, there are 16 VLAN-based port isolation configurations supported in the RTL9303. Each configuration can specify the VLAN ID, Port Mask, and the enable state. The port mask definition of VLAN-based port isolation is different from port-based port isolation. Ports configured as 1 in this port mask could communicate with all ports belonging to the same specified VLAN while ports configured as 0 could only communicate with ports configured as 1 belonging to the same specified VLAN.

7.5. Layer 2 Multicast and IP Multicast

There are two IP multicast frame types supported in RTL9303: IPv4 multicast and IPv6 multicast.

An IPv4 multicast frame must satisfy two conditions:

- The type must be IPv4
- DIP must be in the range of IP Class D [224.0.0.0~239.255.255.255]

An IPv6 multicast frame must satisfy two conditions:

- The type must be IPv6
- The highest two octets of DIP is 0xFF

A packet is deemed a L2 multicast packet if it is not an IP multicast packet and DMAC [40]=1.

The RTL9303 supports IGMPv1/2/3 and MLDv1/2. IGMP/MLD control packets can be trapped to the CPU. Software inserts the IP multicast entry into the L3 or L2 table.

7.6. Reserved Multicast Address

There are some Reserved Multicast Address (RMA) definitions in the IEEE 802.1 standard. The RTL9303 includes 01-80-C2-00-00-00~01-80-C2-00-00-2F and four user defined RMA support. For each RMA, the actions include: Table lookup, Drop, and Trap to CPU. Some of them have options to bypass ingress VLAN filtering and ingress spanning tree filtering if the action is set to ‘Trap to CPU’.

7.7. IEEE 802.1d/1w/1s (STP/RSTP/MSTP)

There are 64 spanning tree instances supported by the RTL9303. The CPU will create a different Port State for different spanning tree instances at each port. The RTL9303 assigns a VID for a received packet, and look up the VLAN table to retrieve the Multiple Spanning Tree Instances (MSTI). Then it follows the port's MSTI state to complete its corresponding ingress/egress check. The Spanning Tree and Rapid Spanning Tree port states are shown below.

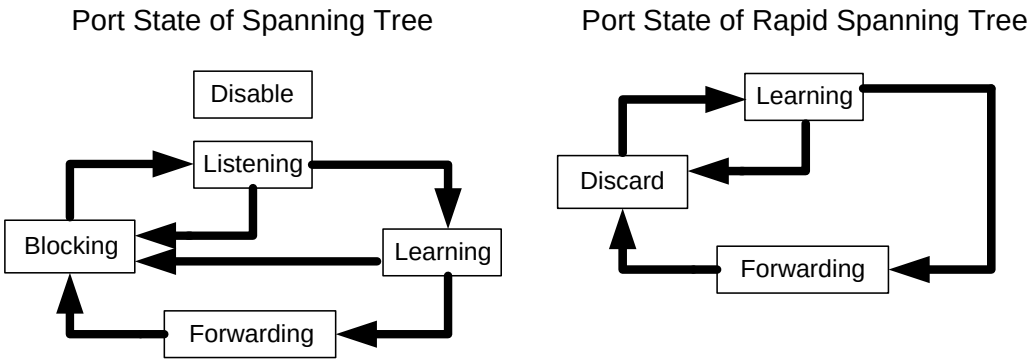


Figure 7. Spanning Tree and Rapid Spanning Tree Port States

When using IEEE 802.1D/1w/1s, the RTL9303 supports four states for each port per instance:

Disable

Except for software forwarding, the port will not transmit/receive packets, and will not perform learning.

Blocking/Listening

Except for software forwarding, the port will only receive BPDU spanning tree protocol packets, but will not transmit any packets, and will not perform learning.

Learning

The port will receive any packet, including BPDU spanning tree protocol packets, and will perform learning, but will only transmit BPDU spanning tree protocol packets.

Forwarding

The port will transmit/receive all packets, and will perform learning.

7.8. IEEE 802.1Q and Q-in-Q VLAN

The RTL9303 has a 4K-entry VLAN table that is used by 802.1Q and Q-in-Q VLAN. Up to three layer VLAN tags (Outer Tag, Inner Tag, Extra Tag) are supported for Q-in-Q applications. The device supports four outer TPIDs, four inner TPIDs and one extra TPID which are all configurable and per port has a TPID mask to select the recognized TPID. For VLAN tag manipulation, VLAN untag set and the egress port tag status configurations are coordinated for determining the tag status for a packet.

Per ingress port can specify the forwarding VLAN is either from inner tag or outer tag. Forwarding VLAN is used for doing VLAN table lookup and ingress/egress VLAN filtering. In Q-in-Q application, outer VLAN ID is used as forwarding VLAN ID for both downlink and uplink ports as well as the inner VLAN ID is used in traditional VLAN application.

The RTL9303 also supports eight protocol-based, 1K MAC-based/IP-subnet-based, and application-based VLANs.

7.9. Ingress and Egress VLAN Translation

The RTL9303 supports 1K ingress and 512K egress VLAN translation table. They are used to support the 1:1 and port-based N:1 VLAN translation. For MAC-based N:1 VLAN translation, per egress port has a configuration to enable the function. In addition to the dedicated VLAN translation tables, VLAN translation can also be done by ACL.

7.10. IEEE 802.3ad Link Aggregation

The RTL9303 supports 802.3ad (Link Aggregation) for 64 groups of link aggregators with up to 8 ports per-group. Link aggregation group frames are sent to one port of the link aggregation group according to a distribution algorithm. Four trunk distribution algorithms are supported and per group can bind to a specific distribution algorithm.

The parameters of the distribution algorithms for L2 and IP packet are independently configured:

- SPP (Source Physical Port), SMAC, DMAC, VLAN-ID are for L2 known unicast packets
- SPP, SMAC, DMAC, VLAN ID, SIP, DIP, L4 source port, L4 destination port, Protocol ID, and IPv6 Flow Label are for L3 known unicast packets

For L2 non-unicast packets it is fixed (SPP, SMAC, DMAC). For L3 non-unicast packets it is (SPP, SIP, DIP).

Each trunk group can optionally separate the known multicast and flooding traffic to the MSB port. H/W fail-over is supported to prevent forwarding traffic to a link down port.

7.11. Mirroring and Sampling

There are 4 mirror configurations supported in the RTL9303. Each mirror configuration can specify the ingress and egress mirrored ports, mirroring port, isolation state, and enable state. Normal forwarding packet cannot be forwarded to the mirroring port if isolation state is enabled. The mirrored traffic can cross the VLAN, that is, the mirrored port and mirroring port can reside in different VLANs.

Multiple mirrored ports are matched for a multiple egress port packet; the packet transmitted through the lowest mirrored port ID is duplicated to the mirroring port. The mirroring port drops the mirrored traffic instead of triggering the flow control if it is congested.

The RTL9303 supports ingress and egress port sFlow sampling. Each ingress and egress port can specify the sample rate for packet sampling and a corresponding trap reason is carried when the packet is sampled to CPU.

Flow-based mirroring and sampling can be supported by ACL.

7.12. Attack Prevention

Most common attacks can be blocked by the RTL9303 including LAND attack, UDP Blat attack, TCP Blat attack, Ping of Death attack, Smurf attack, TCP NULL scan, and so on. The attack prevention function is per port enabled and each attack type is globally enabled except when invalid ARP is per port enabled. Each attack type packet can be selected to drop or trap to CPU for further processing.

7.13. PIE (Packet Inspection Engine)

The Packet Inspection Engine (PIE) performs per-flow processing of packets at wire speed. It is a 2K search engine that is divided into 16 blocks (block numbers are 0~15). Each block contains 128 entries. The PIE consists of VLAN ACL and ingress ACL 2 lookup phase. Each block has a register to configure which phase the block is. VLAN ACL is before ingress VLAN filter and Layer 2 table lookup; ingress ACL is after Layer 2 table lookup.

The PIE has a metadata field that supports OpenFlow application.

7.13.1. VLAN ACL

The VLAN ACL function supports packet drop/permit/redirect/copy to CPU, log, mirror, policing, ingress inner VLAN translation, ingress outer VLAN translation, priority assignment, CPU QID assignment, tag priority remarking, tag status assignment, DSCP remarking, and bypass dropping, metadata and loopback, and IP Reserved Flag Invert functionalities. When a PIE memory block is configured to VLAN ACL, it will execute the corresponding actions when a packet hits the entry.

Each VLAN ACL entry corresponds to multiple actions. When a multi-match occurs (i.e., there are several ACL entries that match), these matched actions will be divided into different action groups. Each group will then execute the lowest address entry corresponding action.

7.13.2. Ingress ACL

The Ingress ACL function supports functionalities similar to VLAN ACL. Differences between them are mainly determined by their lookup phase. For example, Inner VLAN translation function of VLAN ACL translates a packet before the ingress VLAN filter/L2/L3 process, but the function of ingress ACL is after the ingress VLAN filter/L2/L3 process.

7.13.3. Log Counter

The RTL9303 supports 2K 64-bit log counters. Each entry has one counter; it could be set as byte-based or packet-based. Counters belonging to different blocks can be increased concurrently, thus, up to 16 counters can be increased concurrently. One limitation is that VLAN and ingress ACL cannot share the same counter block.

7.14. L3 Unicast and Multicast Routing

Layer 3 routing supports IPv4 and IPv6 protocols. Routing is the process of forwarding packets hop by hop on layer3, it primarily includes finding an outgoing interface and a next hop, modifying the packets' SMAC, DMAC, VID (if provided), TTL and L3 header checksum (for IPv4), and forwarding. L3 routing performs the source/destination IP lookups for IPv4 and IPv6 unicast and multicast packets.

7.14.1. IP Unicast Routing

L3 termination is initiated via a lookup in the Router MAC table. The L3 Host Routing Table is a 2-left 6-way host table, supports max 6K IPv4 entries or 3K IPv6 entries. When a look miss in the L3 host table LPM (Longest Prefix Match) table lookup occurs, it supports 512 IPv4 entries or 128 IPv6 entries. Once matched, a L3_NEXT_HOP entry is used to modify the packets, including outgoing interface and DMAIDX , and fully supports 2K next hop.

The Outgoing interface provides the packets' SMAC, VID etc. information, and includes 128 interfaces. The DMAC and the outgoing port information should be retrieved from an L2 entry indexed by DMACIDX.
Values in the MAC field of the L2 entry indicate the next hop's MAC address, and are used to replace the packets' DMAC field in the L2 header.

IP unicast routing supports Strict and loose uRPF checks and PBR (Policy-Based Routing).

7.14.2. IP Multicast Routing

The RTL9303 supports IGMP/MLD snooping, MVR, PIM-SM, PIM-DM, PIM-SSM, DVMRP, and MOSPF.

IP multicast packets can be routed and bridged at the same time. IP multicast supports two bridge modes: MAC-Based and IP-Based mode. The IP multicast table is shared with the IP unicast host table; with max 2K IPv4 multicast entries or 1K IPv6 multicast entries.

The IP multicast routing table will be searched twice, each time with a different key. In round one, the key used to look is < SIP, DIP, VID (optional) >. In round two, the key is <SIP (set as all 1s), DIP, VID (optional) >. Once the IP multicast packets are determined to be sent to the L3 routing engine (according

to the routing ability and packets' attribute), they are seen as duplicated and sent both to the L2 bridging logic and L3 routing logic.

IP multicast supports L2 only, L3 replication, L2+L3 replication. Max 512 L3 OIL (Outgoing Interface List) list for IPMC replication.

7.15. Traffic Suppression

The priority sequence for traffic suppression is:

1. VLAN ACL policing
2. Ingress bandwidth control
3. Storm control
4. Ingress ACL policing

7.15.1. Ingress Bandwidth Control

The RTL9303 supports ingress bandwidth control configuration for each port. The bandwidth setting ranges from 16Kbps~10Gbps. The granularity is 16Kbps, and each port has a 20-bit register to control the bandwidth. If the receiving packet rate is faster than the bandwidth setting, it can optionally send a 'Pause ON' packet to slow the link partner transmissions. For out of profile detection, per port supports an EXCEED flag to indicate whether the traffic rate was ever over the bandwidth setting.

7.15.2. ACL Policing

The RTL9303 supports 256 policers, which are divided into 16 blocks. Policers belonging to different blocks can be executed concurrently, thus, up to 16 policers can be executed concurrently to support hierarchy policing. The policer support PPS (Packet-Per-Second) and BPS (Bit-Per-Second) two mode, BPS mode rate ranges from 16Kbps~10Gbps with 16Kbps granularity, PPS mode granularity is 1PPS.

Each ACL entry has an index to point to 256 ACL policers. One limitation is that VLAN and ingress ACL cannot share the same policer block.

7.15.3. Storm Control

The per-port L2 storm filtering control mechanism suppresses the flow rate of storm packets. The RTL9303 supports five control types: Unknown Unicast, Unicast, Unknown Multicast, Multicast, and Broadcast Storm. The definitions of five traffic types are:

- Unknown Unicast: If the I/G bit of DMAC address (DMAC[40]) is 0, it is an unicast packet. The failure in L2 unicast table DA look-up is what called "Unknown Unicast".
- Unicast: If the I/G bit of DMAC address (DMAC[40]) is 0, it is an unicast packet.
- Unknown Multicast: If the I/G bit of DMAC address (DMAC[40]) is 1, it is a multicast packet. The failure in L2 multicast table DA look-up or L3 table IP look-up is what called 'Unknown Multicast'.
- Multicast: The success of L2 multicast table DA look-up for a multicast packet is called the 'Known Multicast'. System's Multicast Storm Filtering Control includes Unknown and Known Multicast.

- Broadcast: DMAC = FF-FF-FF-FF-FF-FF is called the ‘Broadcast packet’.

The traffic rate for these five types can be set on a per-port basis and per port per control type supports a EXCEED flag to indicate whether the traffic rate ever overran. PPS (Packet-Per-Second) or BPS (Bit-Per-Second) counting mode can be selected by port.

7.16. Priority Decision

There are eight types of priority decision source for the RTL9303:

- Port
- VLAN ACL
- DSCP
- Inner Tag
- Outer Tag
- MAC-based/IP-subnet-based VLAN
- Protocol-VLAN
- Routing

Each receiving packet will be given an internal priority, and the packet is then en-queued to the output queue according to its internal priority. The internal priority is from one of the eight priority sources. Each priority source has a weight configuration; the priority source with larger weight is taken as the internal priority.

7.17. Packet Scheduling

The Packet Scheduler controls the multiple traffic classes (i.e., controls the packet sending sequence of the priority queue). The RTL9303 scheduling algorithm is divided into Strict Priority (SP), Weighted Fair-Queuing (WFQ) and Weighted Round-Robin (WRR). Note that the Strict Priority queue is the highest priority of all queues, and overrides WFQ & WRR. A larger strict priority queue ID indicates the priority is higher.

The Scheduler operates as follows:

- Strict Priority (SP)
- Weighted Fair-Queuing (WFQ): Byte-count
- Weighted Round-Robin (WRR): Packet-count

WFQ and WRR cannot exist at the same time. Both WFQ and WRR are round robin, from large queue ID to small. Egress bandwidth control supports port-based and queue-based; normal port egress bandwidth unit is 16Kbps.

The CPU port supports both BPS and PPS rate limits. There are Maximum, Fixed, and Assured modes for normal port queue-based egress bandwidth control. Fixed and Assured has a higher bandwidth allocation priority than WFQ/WRR.

Normal ports and the CPU port have different egress queues; there are 8 and 32 queues, respectively.

7.18. Egress Packet Remarking

RTL9303 Remarking can be divided into inner 1p, outer 1p, DSCP, and DEI Remarking. Per egress port per type supports a configuration to turn on the remarking function. For inner 1p Remarking, the remarking source can be from internal priority, original inner 1p priority, original outer 1p priority and DSCP. For outer 1p Remarking, the remarking source is the same as inner 1p Remarking. For DSCP Remarking, it has two additional remarking sources: Drop Precedence (DP), and DP + internal priority.

7.19. IEEE 802.3x Flow Control

The RTL9303 supports IEEE 802.3x full duplex flow control. If the packet buffer used by a port is over the pause threshold, a pause-on frame is sent to indicate to the link partner to stop the transmission. When the frame buffer used by a port drops below the pause threshold, it sends a pause-off frame. The Tx pause frame format is shown below.

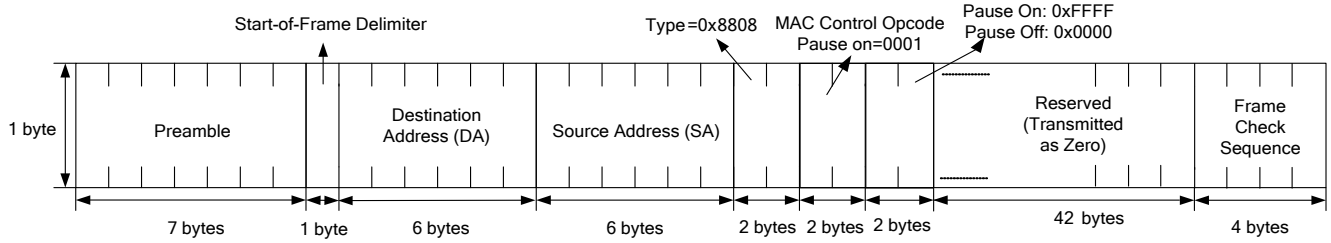


Figure 8. Tx Pause Frame Format

The flow control mechanism of the RTL9303 is implemented on the Ingress side. It counts the received pages on the Ingress side in order to determine on which port it should send out pause on/off packets. Figure 9 shows the flow control state machine.

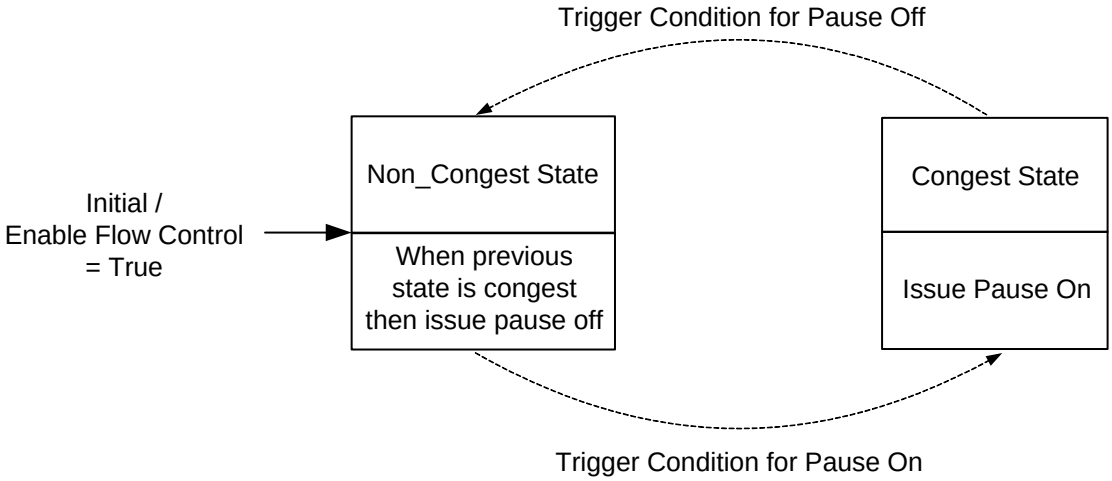


Figure 9. Flow Control State Machine

The first flow control state is 'Non_Congest'. This is continuously monitored for the pause-on trigger condition, at which point it enters the 'Congest' state. In the congest state, it is continuously monitored for the pause-off trigger condition, at which point it re-enters the 'Non_Congest' state.

7.20. Half Duplex Backpressure

There are two mechanisms for half duplex backpressure (Backpressure is for input buffer overflow).

7.20.1. Collision-Based Backpressure (Jam Mode)

If the input buffer used by a ingress port over the configured threshold, this mechanism will force a collision. When the link partner detects this collision, the transmission is rescheduled.

The Reschedule procedure is:

- When the link partner detects the collision, it waits for a random backoff time. The RTL9303 will handle packets that are in the input packet buffer during this time.
- RXDV and TXEN will be driven to high. The RTL9303 will send a 4-byte Jam signal (pattern is 0xAA). Then the RTL9303 will drive TXEN to low.
- When the link partner receives the Jam signal, it will feedback a 4-byte signal.
- The link partner waits for a random backoff time then re-sends the packet.

7.20.2. Carrier-Based Backpressure (Defer Mode)

If the packet buffer used by an ingress port over the configured threshold, this mechanism will send a 2k-bytes defer signal (pattern is 0xAA) to defer the other station's transmission. The RTL9303 will continuously send the defer signal until the packet buffer usage is under the threshold.

7.21. srTCM/trTCM (Single/Two Rate Three Color Marker)

The RTL9303 supports 256 ACL policers which can also be used as srTCM (Single Rate Three Color Marker) and trTCM (Two Rate Three Color Marker).

The srTCM meters a traffic stream and marks its packets according to three traffic parameters, Committed Information Rate (CIR), Committed Burst Size (CBS), and Excess Burst Size (EBS), to be either green, yellow, or red. A packet is marked green if it does not exceed the CBS, yellow if it does exceed the CBS, but not the EBS, and red otherwise.

The trTCM meters a traffic stream and marks its packets based on two rates, Peak Information Rate (PIR) and Committed Information Rate (CIR), and their associated burst sizes to be either green, yellow, or red. A packet is marked red if it exceeds the PIR. Otherwise it is marked either yellow or green depending on whether it exceeds or does not exceed the CIR.

The 256 ACL policers are divided into 16 blocks. Each entry can specify the counting mode to be either PPS (Packet-Per-Second) or BPS (Bit-Per-Second) and configurations includes policer type, PIR rate, CIR rate, and color aware mode.

The packet is marked a color by srTCM/trTCM and the color is then referenced by SWRED to perform egress random dropping for congestion avoidance.

7.22. SWRED (Simple Weighted Random Early Detection)

When SWRED is not configured, output buffers fill during periods of congestion. When the buffers are full, tail drop occurs; all additional packets are dropped. Since the packets are dropped all at once, global synchronization of TCP hosts can occur as multiple TCP hosts reduce their transmission rates. The congestion clears, and the TCP hosts increase their transmissions rates, resulting in waves of congestion followed by periods where the transmission link is not fully used.

SWRED reduces the chances of tail drop by selectively dropping packets when the output interface begins to show signs of congestion. By dropping some packets early rather than waiting until the buffer is full, SWRED avoids dropping large numbers of packets at once and minimizes the chances of global synchronization. Thus, SWRED allows the transmission line to be used fully at all times.

The RTL9303 SWRED provides separate thresholds and weights for different drop precedence (0: Green, 1: Yellow, 2: Red), allowing you to provide different qualities of service for different traffic. It simplifies the calculation of packet marking probability as shown in Figure 10.

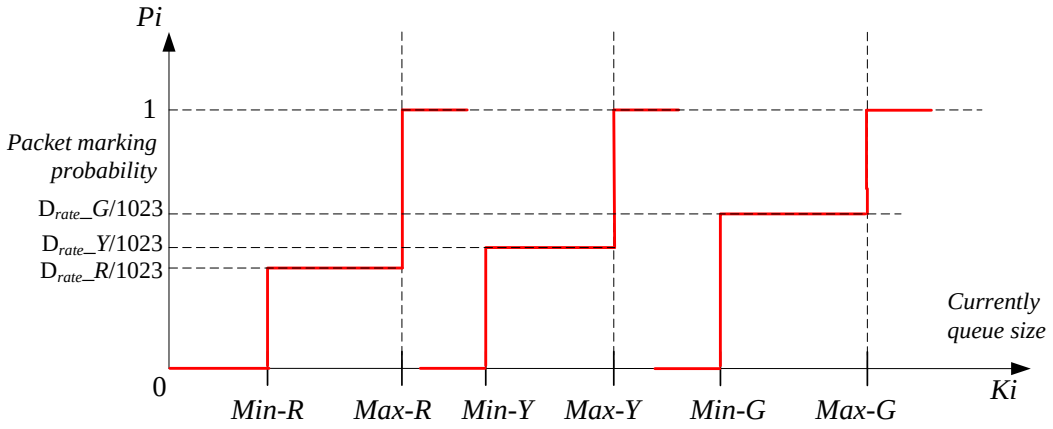


Figure 10. SWRED Packet Marking Probability of Different Drop Precedence

7.23. Management Information Base (MIB)

The supported MIB (Management Information Base) counters include:

- Ethernet-like MIB (RFC 3635)
- Interface Group MIB (RFC 2863)
- RMON (Remote Network Monitoring) MIB (RFC 2819)
- Bridge MIB (RFC 1493)
- Bridge MIB Extension (RFC 2674)
- TCP/IP-based MIB-II (RFC 1213)
- Private MIB counter

7.24. NIC and CPU Tag Forwarding

The NIC interface is used for receiving packets from the CPU, or transmitting packets to the CPU. The architecture is shown below.

When a packet is sent from the switch core to the CPU port, the CPU tag can carry status information. The CPU tag can be divided into a transmit CPU tag, and a receive CPU tag. The transmit CPU Tag can force the egress port mask. The receive CPU Tag indicates the ingress port the packet came from and the reason why it was sent to the CPU. If no transmit CPU tag is attached, a standard L2 table lookup is taken to forward the packet.

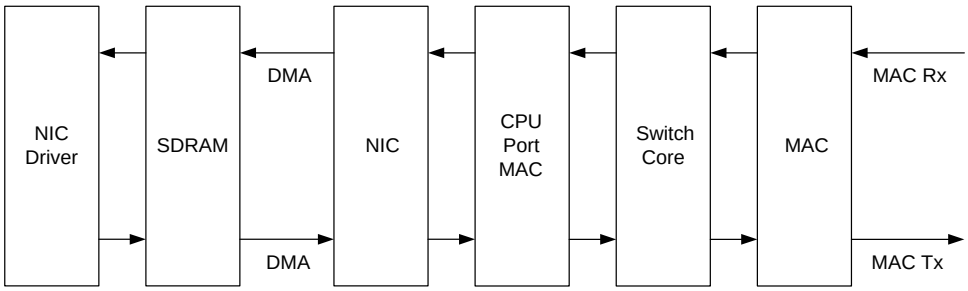


Figure 11. NIC Architecture

7.25. Table Access

The RTL9303 employs an indirect method to set the control register and the data register to complete Layer 2/VLAN/ACL Table Access:

1. Set the register to determine which table and which entry is to be accessed.
2. Determine the read or write operation.
3. Hardware executes table access.

Read: After the control register setup has been completed by software, hardware starts accessing and retrieves the data into the data register. Software then reads this data from the data register.

Write: Software puts the data in the data register and indicates the write operation in the control register. Then hardware writes the data from the data register to the table.

7.26. External PHY Register Access

The RTL9303 supports PHY access control registers to indirectly access an external PHY via the MDC/MDIO interface.

7.27. OAM (Operation, Administration, Maintenance)

IEEE 802.3ah OAM provides mechanisms useful for monitoring link operation such as remote fault indication and remote loopback control. In general, OAM provides network operators the ability to monitor the health of the network and quickly determine the location of failing links or fault conditions.

The OAM loopback function supported by the RTL9303 is wire-speed guaranteed and the source/destination MAC address can be swapped for the loopback packet.

When the system power is lower than a pre-defined voltage, an OAM Dying Gasp message is sent to the administrator for fault indication. Hardware-based Dying Gasp is sent within a very short time, thus, a large volume capacitance can be omitted to save the system cost. The OAM dying gasp application circuit is shown below.

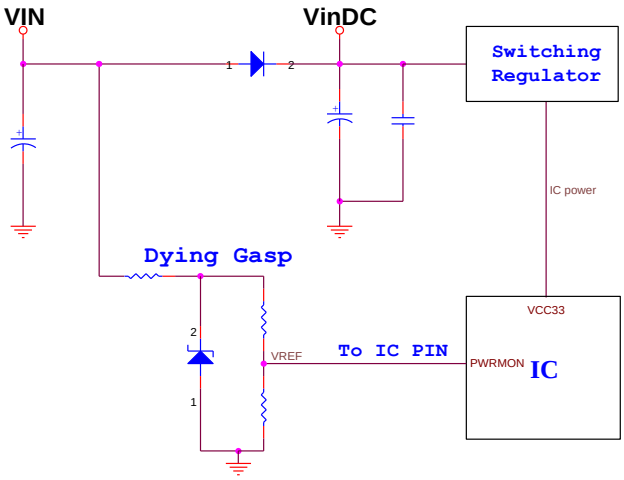


Figure 12. OAM Dying Gasp Application Circuit

7.28. EEE

EEE proposes a low power idle (LPI) mode where the MAC and PHY can shut down parts of electric circuits to reduce power consumption. If there is no traffic to be transmitted, the TX part of a port can enter LPI mode to sleep. If the link partner enters TX LPI mode, the connected port can enter RX LPI mode.

The RTL9303 per port can enable the TX/RX EEE function separately for different link speeds (excluding 10Mbps).

8. CPU Function Description

8.1. MIPS-34Kc

- CPU Core
  - Up to 800MHz
  - 9-stage pipeline
  - MIPS32 and additional MIPS16e instruction set support
- Cache Configuration
  - 32KB I-Cache
  - 32KB D-Cache
- MMU Configuration
  - 4-entry ITLB
  - 4-entry DTLB
  - 32-entry JTLB

8.2. SPI Flash Controller

The RTL9303 supports both SPI NOR and SPI NAND Flash.

SPI NOR specification below:

- Two chip select with up to 32MB (3-byte mode), 64MB (4-byte mode)
- Serial/Dual/Quad data width
- Programmed I/O interface and memory-mapped I/O interface for read operation is supported
- Cached read access

SPI NAND specification is below:

- Two chip select with up to 512MB
- Serial/Dual/Quad data width
- PIO and DMA data read/write operation is supported
- Configurable flash access timing

8.3. DDR Memory Controller

DDR3 are supported with the specification below.

- 8/16 bit bus width
- Low speed DDR3 up to 800MHz (DDR3-1600)
- Up to 1GB

9. Electrical AC/DC Characteristics

9.1. Absolute Maximum Ratings

WARNING: Absolute maximum ratings are limits beyond which permanent damage may be caused to the device, or device reliability will be affected. All voltages are specified reference to GND unless otherwise specified.

Table 15. Absolute Maximum Ratings

Parameter	Min	Max	Units
Junction Temperature (Tj)	-	+125	°C
Storage Temperature	-10	+125	°C
DVDDH, SVDDH Supply Referenced to GND and SGND	2.97	3.63	V
AVDDH_PLL, AVDDH_CEN, AVDDH_XTAL Supply Referenced to	2.97	3.63	V
AVDDH_USB Supply Referenced to GND	2.97	3.63	V
DVDDL, SVDDL Supply Referenced to GND and SGND	0.99	1.21	V
AVDDL_PLL, AVDDL_CEN, AVDDL_DLL Supply Referenced to GND	0.99	1.21	V
AVDDL_CK Supply Referenced to GNDCK3/2/1/0	0.99	1.21	V
AVDDL_USB Supply Referenced to GND	0.99	1.21	V
MVDDH Supply Referenced to GND (for DDR3)	1.35	1.65	V
DVDDIO_G4/3/2/1 Supply Referenced to GND (for GPIO)	2.97	3.63	V
	2.25	2.75	V
DVDD_MDX3/2/1/0 Supply Referenced to GND (for MDX Circuit)	2.97	3.63	V
	1.0	1.5	V

9.2. Recommended Operating Range

Table 16. Recommended Operating Range

Parameter	Min	Typ	Max	Units
Ambient Operating Temperature (Ta)	0	-	70	°C
DVDDH, AVDDH_PLL, AVDDH_CEN, AVDDH_XTAL, SVDDH Supply Voltage Range	3.135	3.3	3.465	V
DVDDL, AVDDL_PLL, AVDDL_CK, AVDDL_CEN, AVDDL_DLL, SVDDL Supply Voltage Range	1.05	1.1	1.15	V
MVDDH Supply Voltage Range (for DDR3)	1.425	1.5	1.575	V
AVDDH_USB Supply Voltage Range (for USB)	3.135	3.3	3.465	V
AVDDL_USB Supply Voltage Range (for USB)	1.05	1.1	1.15	V
DVDDIO_G4/3/2/1 Supply Voltage Range (for GPIO)	2.375	2.5	2.625	V
	3.135	3.3	3.465	
DVDD_MDX3/2/1/0 Supply Voltage Range (for MDX Circuit)	3.135	3.3	3.465	V
	1.0	1.2	1.5	V

9.3. DC Characteristics

Table 17. DC Characteristics (DVDD33=3.3V)

Symbol	Parameter	Min	Typ	Max	Units
V_{IH}	LVTTL Input-High Voltage	2.0	-	-	V
V_{IL}	LVTTL Input-Low Voltage	-	-	0.8	V
V_{OH}	Output-High Voltage	2.4	-	-	V
V_{OL}	Output-Low Voltage	-	-	0.4	V

9.4. AC Characteristics

9.4.1. Clock Characteristics

Table 18. XTALI (XI) Characteristics

Parameter	Min	Typ	Max	Units
Frequency of XTALI	-	25	-	MHz
Frequency Tolerance of XTALI	-50	-	+50	ppm
Duty Cycle of XTALI	40	-	60	%
Rise Time of XTALI	-	-	12.5	ns
Fall Time of XTALI	-	-	12.5	ns
Jitter of XTALI	-	-	200	ps

9.4.2. SGMII Differential Transmitter Characteristics

Table 19. SGMII Differential Transmitter Characteristics

Symbol	Parameter	Min	Typ	Max	Units	Notes
UI	Unit Interval	799.94	800	800.06	ps	800ps ± 300ppm
$V_{TX-DIFFp-p}$	Output Differential Voltage	400	700	900	mV	-
$T_{TX-JITTER}$	Output Jitter	-	-	0.375	UI	$T_{TX-JITTER-MAX}$ = 1 - $T_{TX-EYE-MIN}$ = 0.35UI

9.4.3. SGMII Differential Receiver Characteristics

Table 20. SGMII Differential Receiver Characteristics

Symbol	Parameter	Min	Typ	Max	Units	Notes
UI	Unit Interval	799.94	800	800.06	ps	800ps ± 300ppm
$V_{RX-DIFFp-p}$	Input Differential Voltage	200	-	1200	mV	-
T_{RX-EYE}	Minimum RX Eye Width	0.375	-	-	UI	-
R_{RX}	Differential Resistance	80	100	120	ohm	-

9.4.4. 1000Base-X Differential Transmitter Characteristics

Table 21. 1000Base-X Differential Transmitter Characteristics

Symbol	Parameter	Min	Typ	Max	Units	Notes
UI	Unit Interval	799.94	800	800.06	ps	800ps ± 300ppm
$V_{TX-DIFFp-p}$	Output Differential Voltage	400	700	900	mV	-
$T_{TX-JITTER}$	Output Jitter	-	-	0.375	UI	$T_{TX-JITTER-MAX}$ = 1 - $T_{TX-EYE-MIN}$ = 0.35UI

9.4.5. 1000Base-X Differential Receiver Characteristics

Table 22. 1000Base-X Differential Receiver Characteristics

Symbol	Parameter	Min	Typ	Max	Units	Notes
UI	Unit Interval	799.94	800	800.06	ps	800ps ± 300ppm
$V_{RX-DIFFp-p}$	Input Differential Voltage	200	-	1200	mV	-
T_{RX-EYE}	Minimum RX Eye Width	0.375	-	-	UI	-
R_{RX}	Differential Resistance	80	100	120	ohm	-

9.4.6. 10GBase-R Differential Transmitter Characteristics

Table 23. 10GBase-R Differential Transmitter Characteristics

Symbol	Parameter	Min	Typ	Max	Units	Notes
UI	Unit Interval	-	97	-	ps	-
$V_{TX-DIFFp-p}$	Output Differential Voltage	400		1200	mV	-
T_J	Total Jitter	-	-	0.28	UIpp	-
R_{TX}	Transmitter output impedance on chip	-	100	-	ohm	-

9.4.7. 10GBase-R Differential Receiver Characteristics

Table 24. 10GBase-R Differential Receiver Characteristics

Symbol	Parameter	Min	Typ	Max	Units	Notes
UI	Unit Interval	-	97	-	ps	-
$V_{RX-DIFFp-p}$	Input Differential Voltage	200	-	950	mV	-
R_{RX}	Receiver input impedance on chip	-	100	-	ohm	-

9.4.8. DDR3 Characteristics

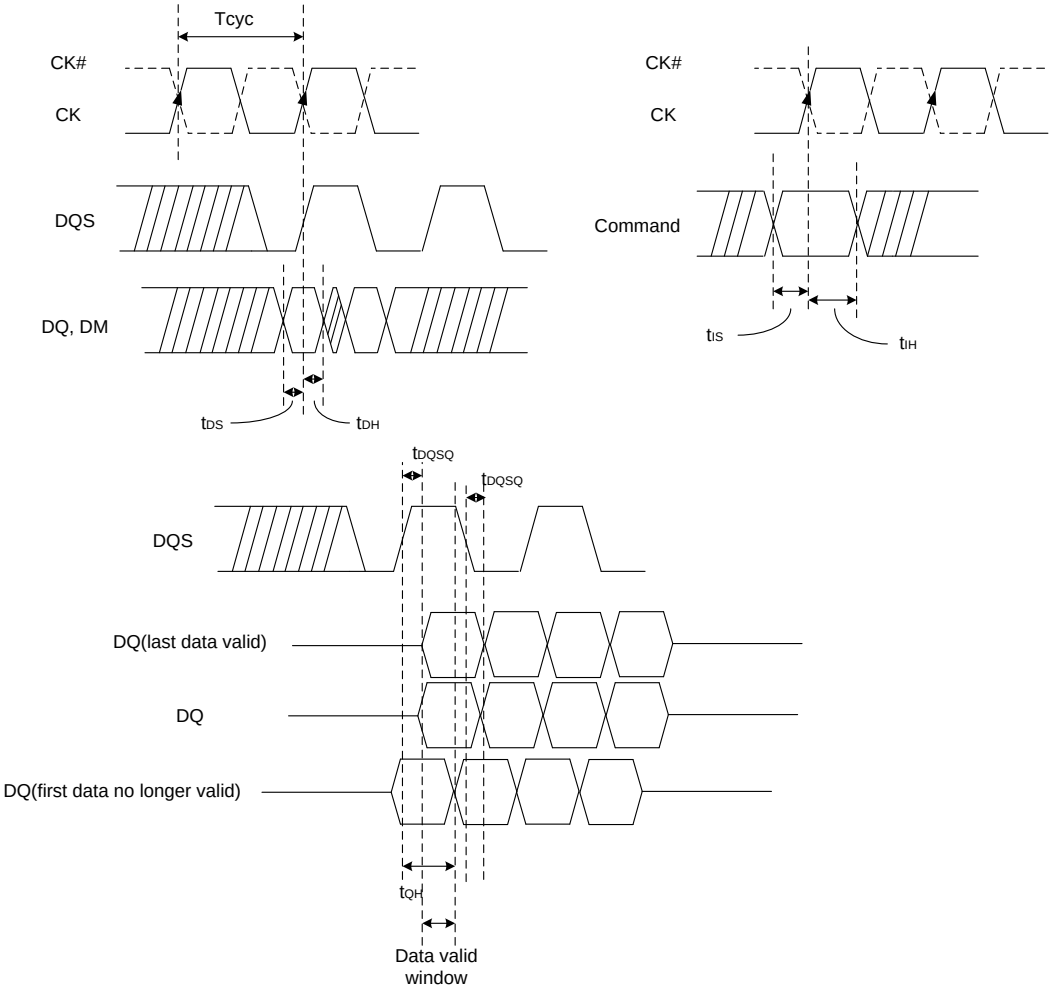


Figure 13. DDR3 Timing

Table 25. DDR3 Timing Characteristics

Symbol	Description	I/O	Min	Typ	Max	Units
f_{CK}, $f_{CK\#}$	Clock Frequency of the CK and CK#	O	-	600	-	MHz
Duty	Duty Cycle of the CK and CK#	O	47	50	53	%
t_{JITper}	Clock period jitter	O	-80	-	80	ps
t_{JITcc}	Cycle-to-cycle jitter	O	-160	-	160	ps
t_{DS}	DQ and DM Output Setup Time	O	30	-	-	ps
t_{DH}	DQ and DM Output Hold Time	O	65	-	-	ps
t_{IS}	Address and Control Output Setup Time	O	190	-	-	ps
t_{IH}	Address and Control Output Hold Time	O	140	-	-	ps
t_{DQSQ}	Input DQS-DQ Skew, DQS to Last DQ Valid	I	-	-	125	ps
t_{QH}	Input DQ-DQS Hold. DQS to first DQ to Go Non-Valid	I	0.38	-	-	ps

9.4.9. SPI Master Controller Interface Characteristics

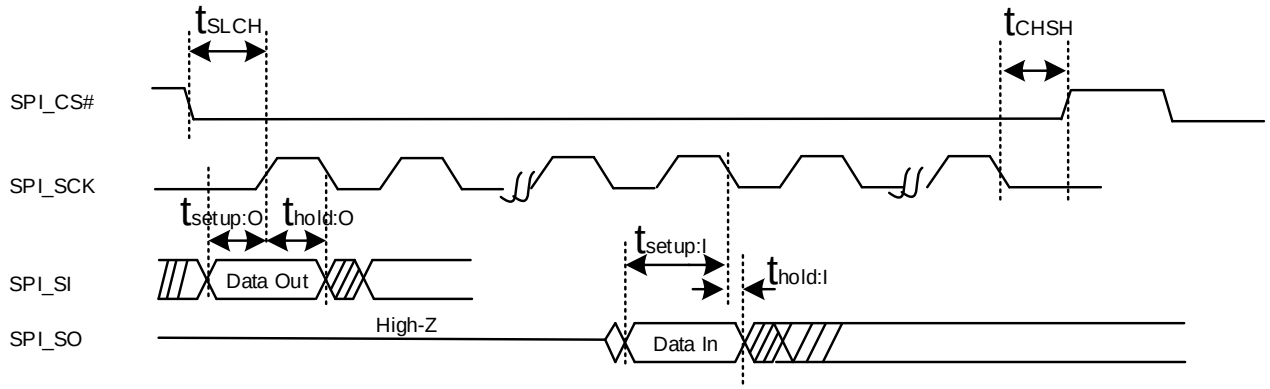


Figure 14. Master SPI Flash Controller Interface Timing

Table 26. Master SPI Flash Controller Interface Timing Characteristics

Symbol	Parameter	Min	Typ	Max	Units
f_{SCK}	Clock Frequency of the SPI_SCK	50.5	51	51.5	MHz
Duty	Duty Cycle of the SPI_SCK	45	50	55	%
t_{SLCH}	CS# Active Setup Time	20	25	-	ns
t_{CHSH}	CS# Active Hold Time	15	20	-	ns
$t_{setup:O}$	Data Output Setup Time	4	8.5	-	ns
$t_{hold:O}$	Data Output Hold Time	6	9	-	ns
$t_{setup:I}$	Data Input Setup Time	4	-	-	ns
$t_{hold:I}$	Data Input Hold Time	0	-	-	ns

9.4.10. SPI Slave Interface Characteristics

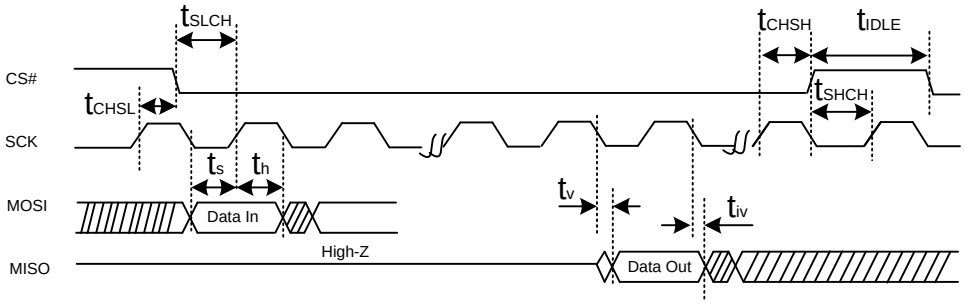


Figure 15. Slave SPI Flash Controller Interface Timing

Table 27. Slave SPI Flash Controller Interface Timing Characteristics

Symbol	Description	Min	Typ	Max	Units
f_{SCK}	Clock Frequency of the SPI_SCK	-	25	50	MHz
t_s	Data Input Setup Time	3	-	-	ns
t_h	Data Input Hold Time	0	-	-	ns
t_v	SCK to MISO valid	-	3.5	5	ns
t_{iv}	SCK to MISO invalid	0	2	-	ns
t_{SLCH}	CS# Active Setup Time	7	-	-	ns
t_{CHSH}	CS# Active Hold Time	7	-	-	ns
t_{SHCH}	CS# Not Active Setup Time	7	-	-	ns
t_{CHSL}	CS# Not Active Hold Time	7	-	-	ns
t_{IDLE}	CS# High Time	7	-	-	ns

9.4.11. EJTAG Timing Characteristics

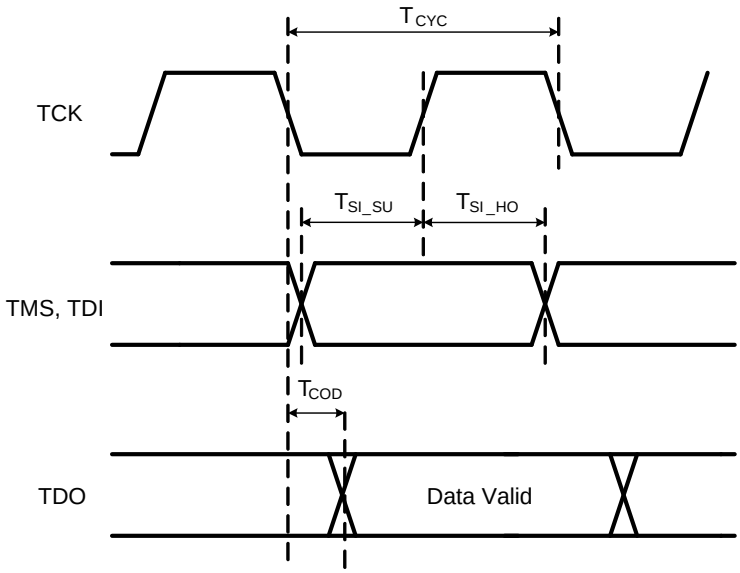


Figure 16. EJTAG Timing

Table 28. EJTAG Interface Timing Characteristics

Symbol	Parameter	I/O	Min	Typ	Max	Units
T_{CYC}	CLK Input Cycle Time	I	20	-	-	ns
T_{SI_SU}	TMS and TDI Setup Times	I	5	-	-	ns
T_{SI_HO}	TMS and TDI Hold Times	I	1	-	-	ns
T_{COD}	TDO Output Delay	O	-	10.4	-	ns

9.4.12. SMI (MDC/MDIO) Interface Characteristics

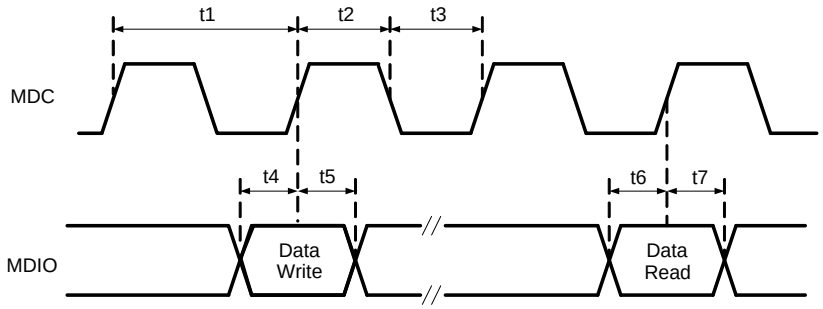


Figure 17. SMI (MDC/MDIO) Timing

Table 29. SMI (MDC/MDIO) Timing Characteristics

Symbol	Description	Min	Typ	Max	Units
t1	MDC Clock Period	-	391.8	-	ns
t2	MDC High Time	-	195.9	-	ns
t3	MDC Low Time	-	195.9	-	ns
t4	MDIO to MDC Rising Setup Time (Write Data)	-	195.9	-	ns
t5	MDIO to MDC Rising Hold Time (Write Data)	-	195.9	-	ns
t6	MDIO to MDC Rising Setup Time (Read Data)	40	-	-	ns
t7	MDIO to MDC Rising Hold time (Read Data)	2	-	-	ns

9.4.13. LED Timing Characteristics

9.4.13.1 Serial LED Mode

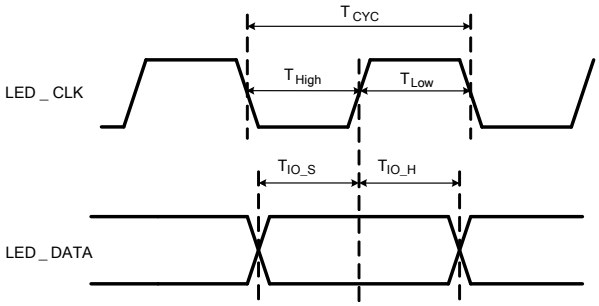


Figure 18. Serial LED Timing

Table 30. Serial LED Timing Characteristics

Symbol	Description	I/O	Min	Typ	Max	Units
T_{CYC}	LED Clock Period	O	-	400	-	ns
T_{High}	LED High Time	O	-	200	-	ns
T_{Low}	LED Low Time	O	-	200	-	ns
T_{IO_S}	LED_DATA to LED_CLK Rising Setup Time	O	-	200	-	ns
T_{IO_H}	LED_DATA to LED_CLK Rising Hold Time	O	-	200	-	ns

9.4.13.2 Scan LED mode

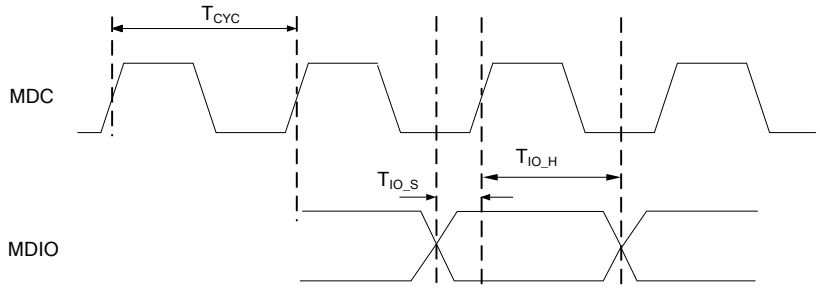


Figure 19. Scan LED timing

Table 31. Scan LED Timing Characteristics

Symbol	Description	I/O	Min	Typ	Max	Units
T_{CYC}	LED Clock Period	O	-	400	-	ns
T_{IO_S}	MDIO to MDC Rising Setup Time	O	-	200	-	ns
T_{IO_H}	MDIO to MDC Rising Hold Time	O	-	200	-	ns

9.4.14. Power and Reset Characteristics

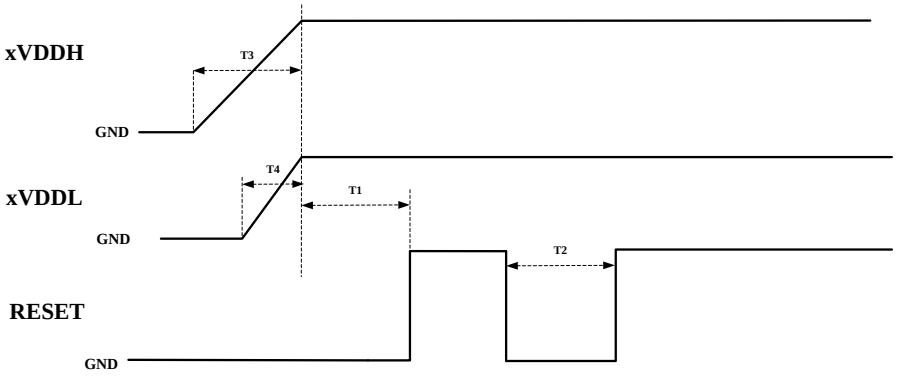


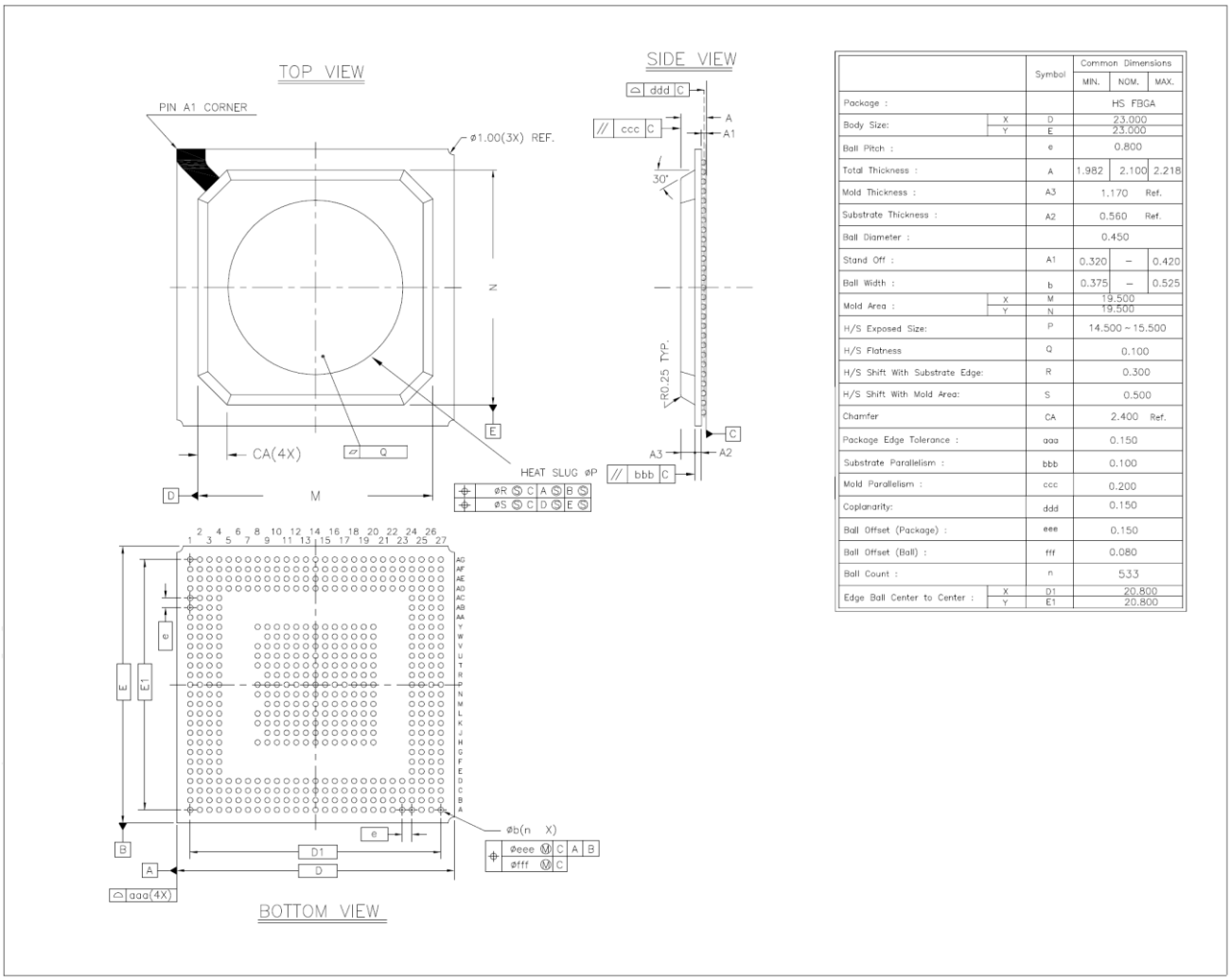
Figure 20. Power and Reset Timing

Table 32. Power and Reset Timing Characteristics

Symbol	Description	Min	Typ	Max	Units
T1	The duration from all of VDDH and all of VDDL power steady to reset signal release to high	10	-	-	ms
T2	The duration of reset signal remain low timing	10	-	-	ms
T3	All of VDDH power rising time	0.5	-	-	ms
T4	All of VDDL power rising time	0.5	-	-	ms

10. Mechanical Dimensions

*10.1. EDHS-PBGA533 (23*23)*



		Symbol	Common Dimensions		
			MIN.	NOM.	MAX.
Package :				HS FBGA	
Body Size:	X	D		23.000	
	Y	E		23.000	
Ball Pitch :		e		0.800	
Total Thickness :		A	1.982	2.100	2.218
Mold Thickness :		A3		1.170 Ref.	
Substrate Thickness :		A2		0.560 Ref.	
Ball Diameter :				0.450	
Stand Off :		A1	0.320	–	0.420
Ball Width :		b	0.375	–	0.525
Mold Area :	X	M		19.500	
	Y	N		19.500	
H/S Exposed Size:		P		14.500 ~ 15.500	
H/S Flatness		Q		0.100	
H/S Shift With Substrate Edge:		R		0.300	
H/S Shift With Mold Area:		S		0.500	
Chamfer		CA		2.400 Ref.	
Package Edge Tolerance :		aaa		0.150	
Substrate Parallelism :		bbb		0.100	
Mold Parallelism :		ccc		0.200	
Coplanarity:		ddd		0.150	
Ball Offset (Package) :		eee		0.150	
Ball Offset (Ball) :		fff		0.080	
Ball Count :		n		533	
Edge Ball Center to Center :	X	D1		20.800	
	Y	E1		20.800	

11. Ordering Information

Table 33. Ordering Information

Part Number	Package	Status
RTL9303-CG	EDHS-PBGA533 (23mm*23mm)	MP

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